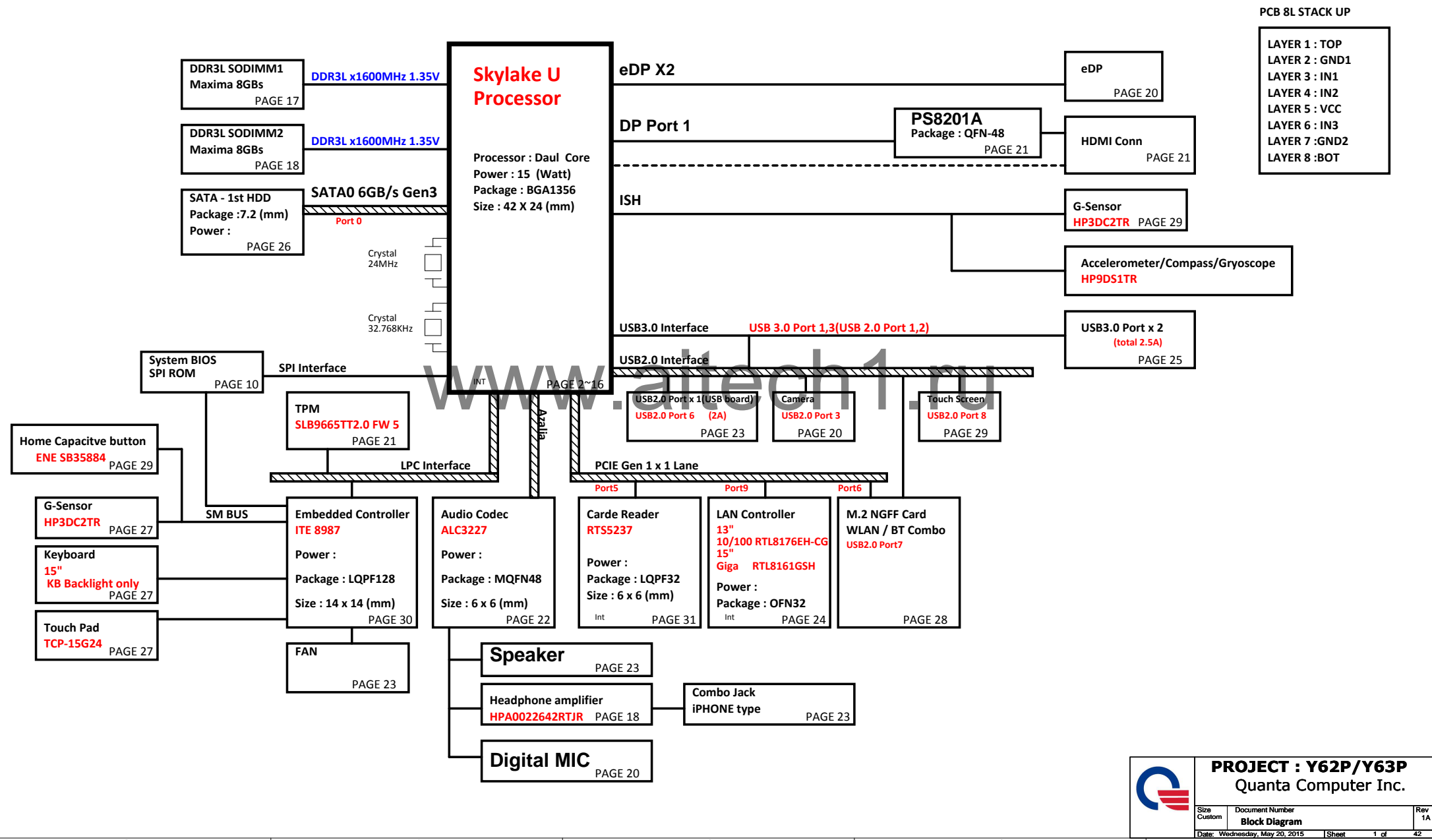


13"/15" Intel Skylake ULT Platform Block Diagram



+3V 4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
 +1.0V 4,6,16,30,36
 +VCCIO 6,16,36
 +VCCSTPLL 4,5,6,9,36,37

HDMI

21 IN_D2# IN_D2# E55
 21 IN_D2 IN_D2# F55
 21 IN_D1# IN_D1# F58
 21 IN_D1 IN_D1# F53
 21 IN_D0# IN_D0# G53
 21 IN_D0 IN_D0# F56
 21 IN_CLK# IN_CLK# G56
 21 IN_CLK IN_CLK# G56

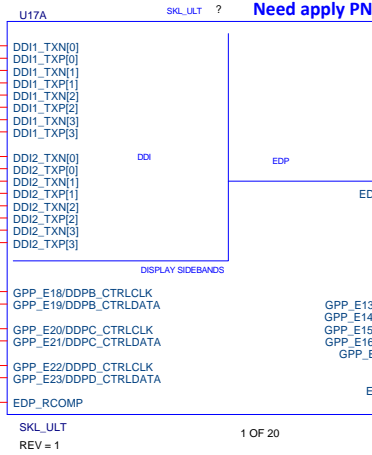
21 SDVO_CLK SDVO_CLK L13
 21 SDVO_DATA SDVO_DATA L12

TP23 DDPC_CTRLDATA N7

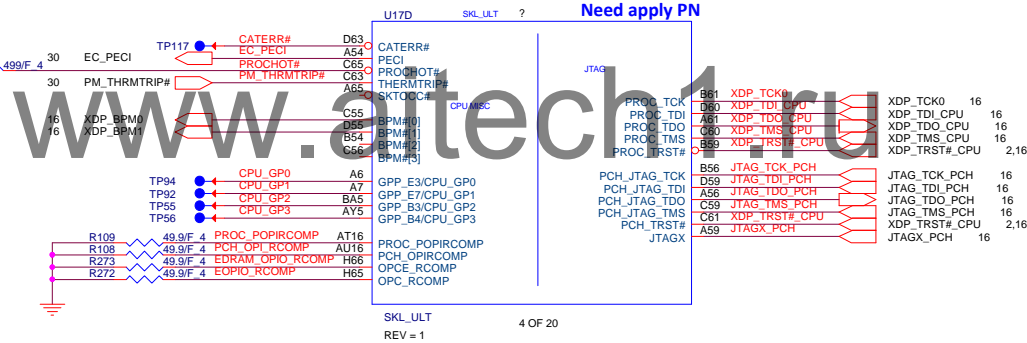
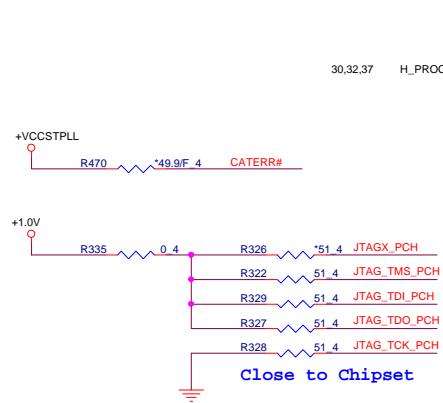
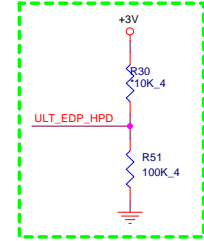
TP21 DDPC_CTRLDATA N11

+VCCIO R220 24.9/F 4 EDP_RCOMP E52

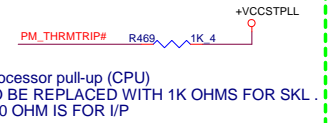
EDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



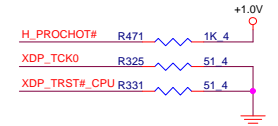
Reserve EDP_HPD opposites circuit!



Close to EC



PLACE NEAR CPU



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Size Custom	Document Number 02 - SKYPAKE 1/20(eDP/DDI)	Rev 1A
Date: Wednesday, May 20, 2015	Sheet 2 of	42

SkyLake ULT Processor (DDR3L)

Need apply PN

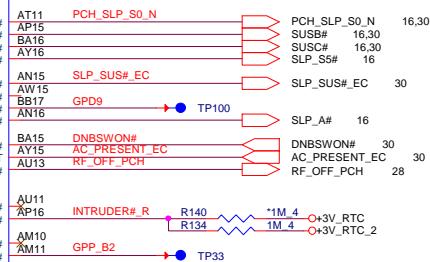
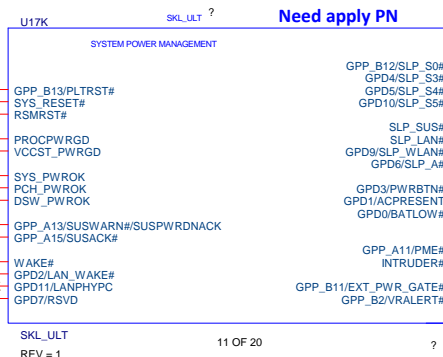
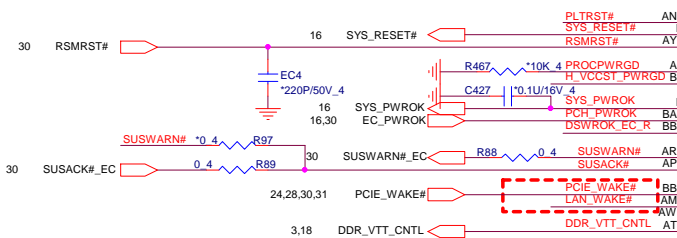
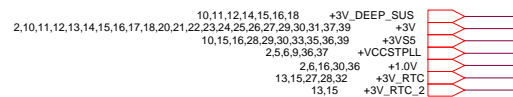
Need apply PN

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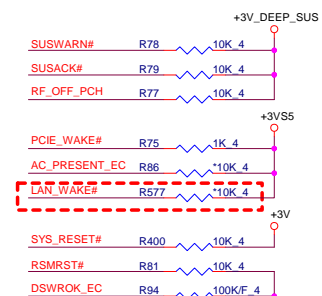


PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	03 - SKYPAGE 3/20(DDR3-A I/F)	
Date: Wednesday, May 20, 2016	Sheet	3 of 42

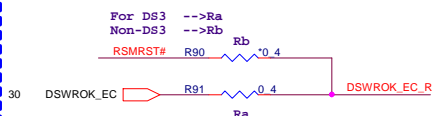


PCH Pull-high/low(CLG)



0508 LAN_WAKE# reserve 10K OHM to +3VS5

For DS3 Sequence

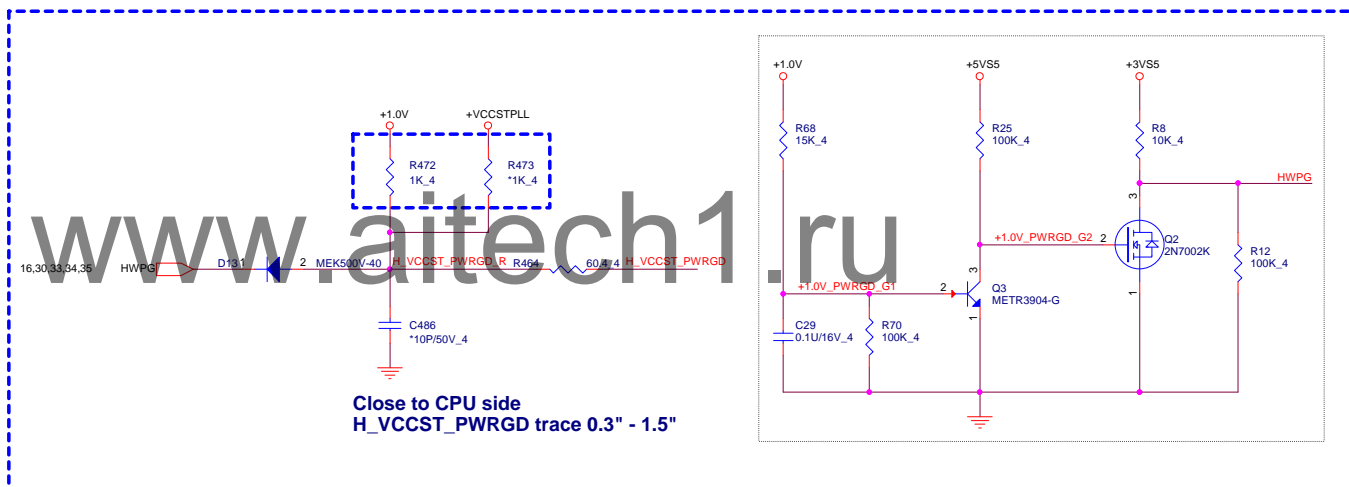
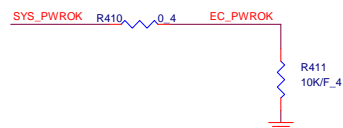


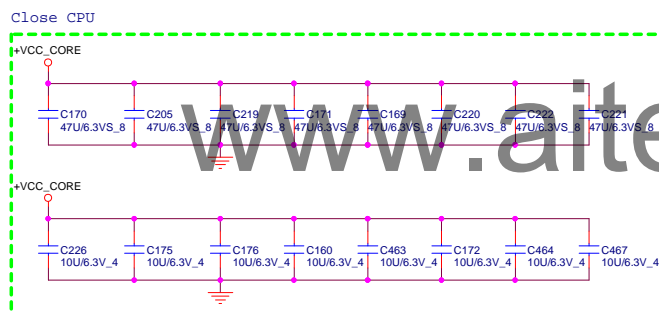
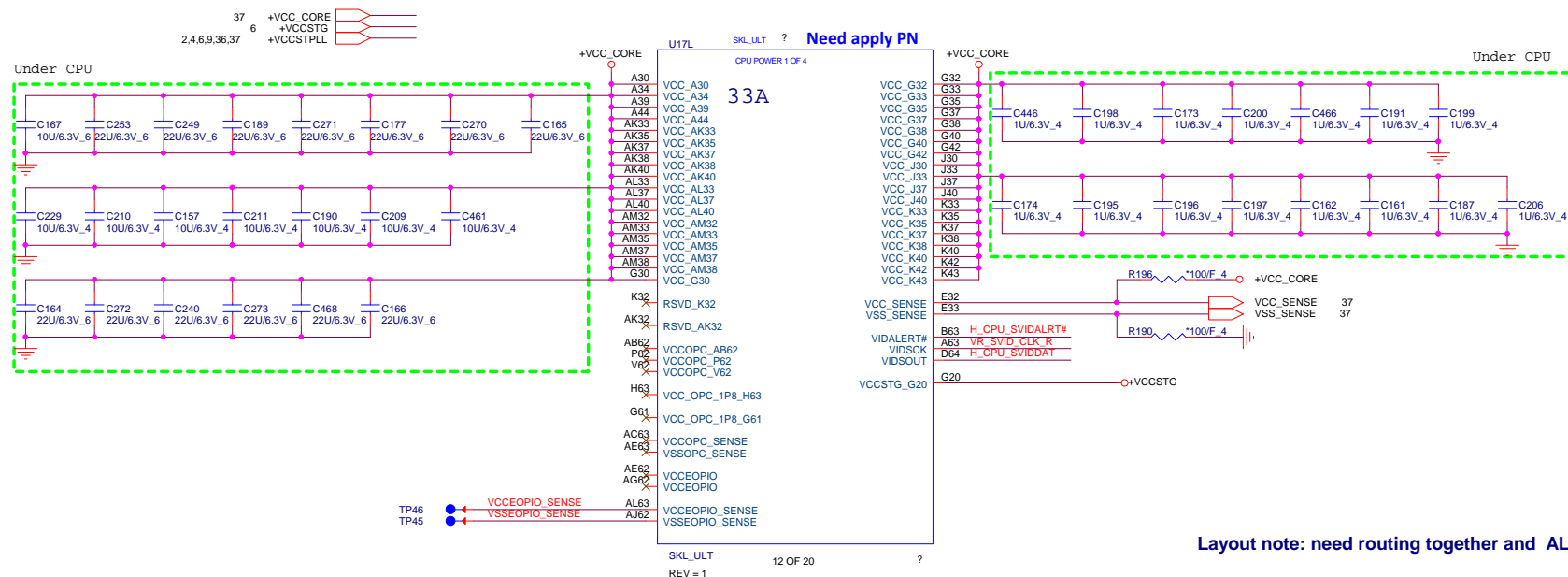
PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns



System PWR_OK(CLG)



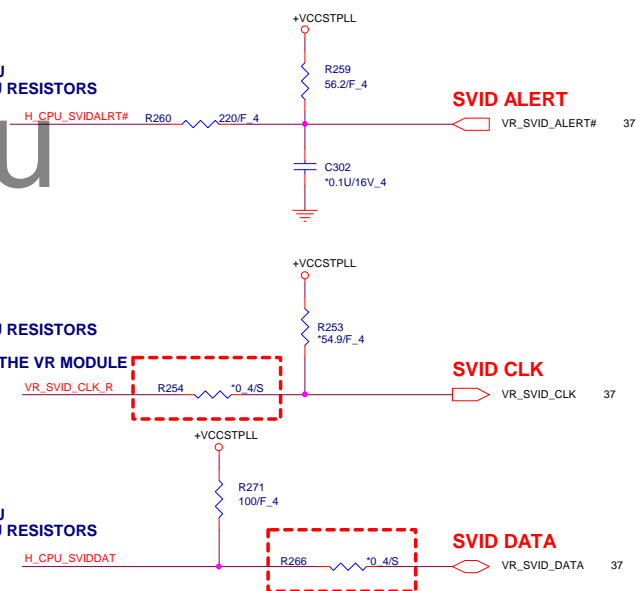


Layout note: need routing together and ALERT need between CLK and DATA.

CLOSE TO CPU
PLACE THE PU RESISTORS

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

CLOSE TO CPU
PLACE THE PU RESISTORS



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

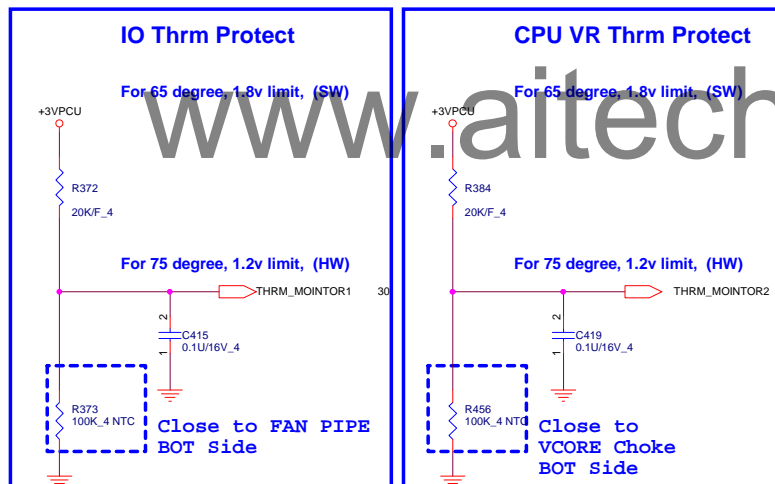
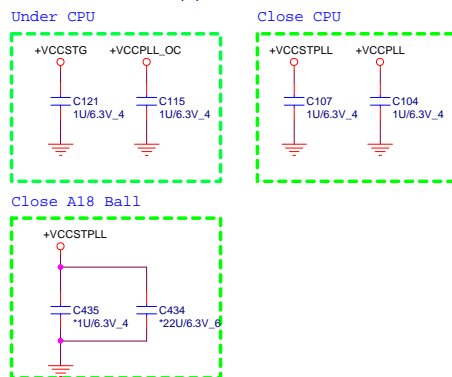
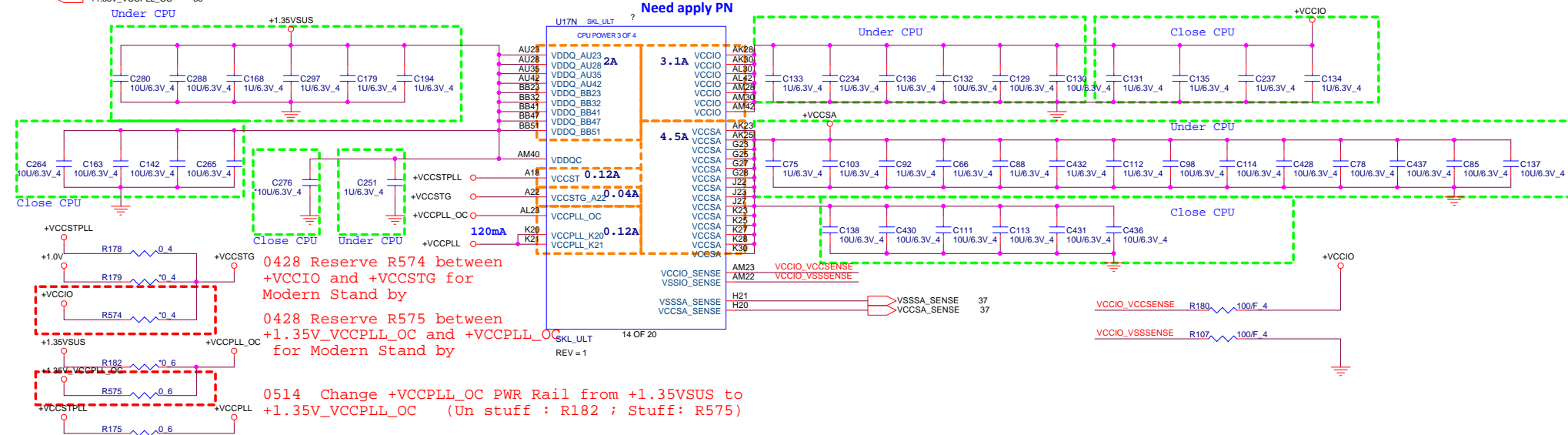


PROJECT : Y62P/Y63P
Quanta Computer Inc.

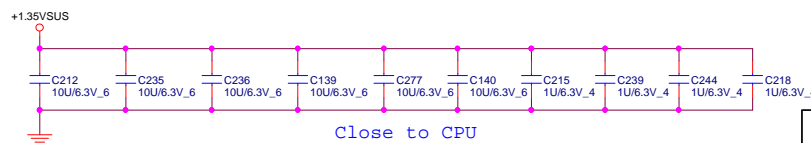
Size	Document Number	Rev
Custom	05 - SKYPAKE 6/20 (POWER-1)	1A
Date: Wednesday, May 20, 2015	Sheet 5 of	42

+VCCSTPLL 2,4,5,9,36,37
 +VCCSA 37,38
 +1.35VSUS 3,17,18,34,36
 +VCCIO 2,16,36
 +1.0V 2,4,16,30,36
 +3VPCU 13,18,27,28,30,32,33
 +1.35V_VCCPLL_OC 36

Need apply PN

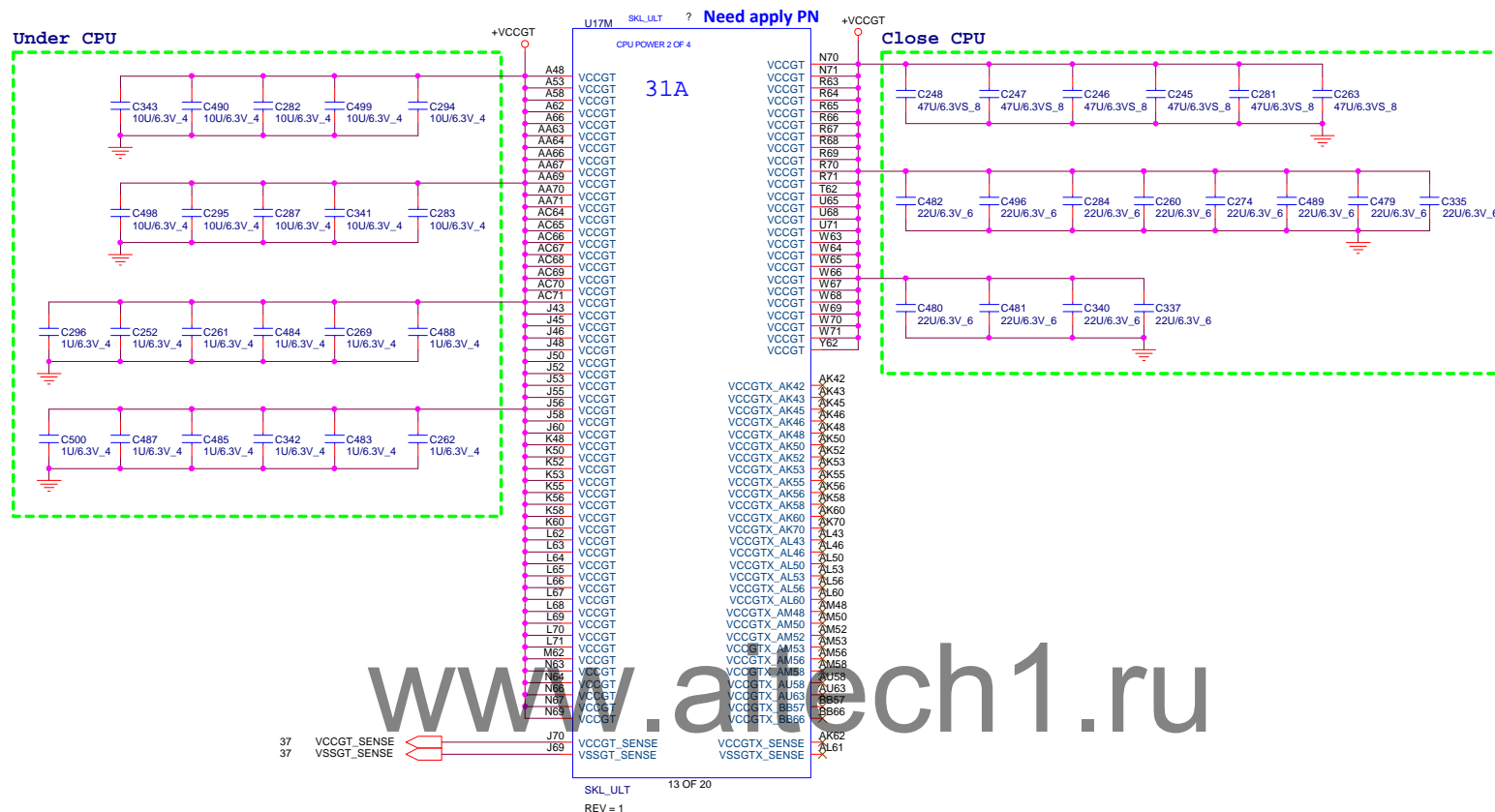


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCePIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

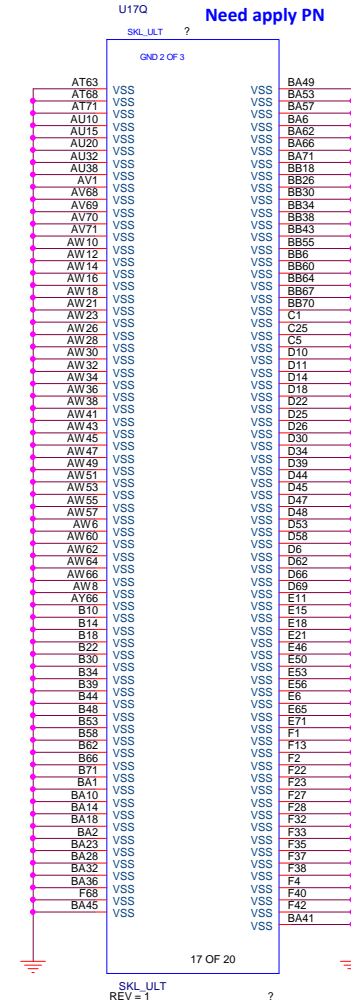
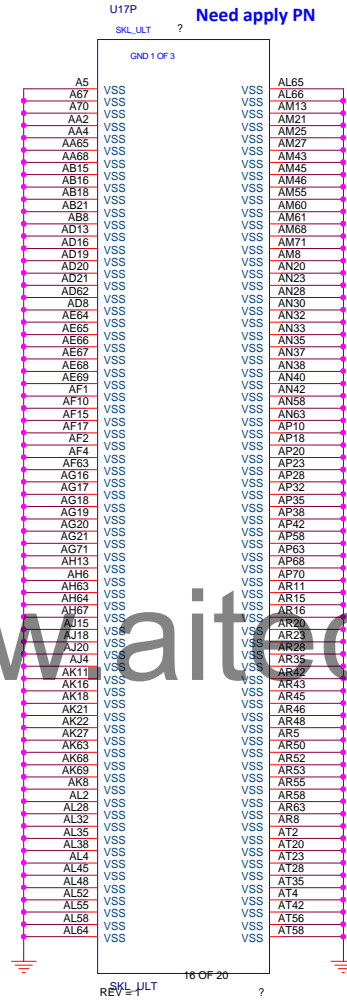
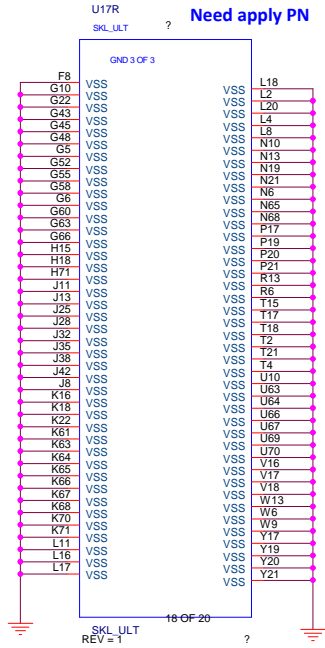


PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size Custom	Document Number 06 - SKYPAKE 7/20 (POWER-2)	Rev 1A
Date: Wednesday, May 20, 2015	Sheet	6 of 42

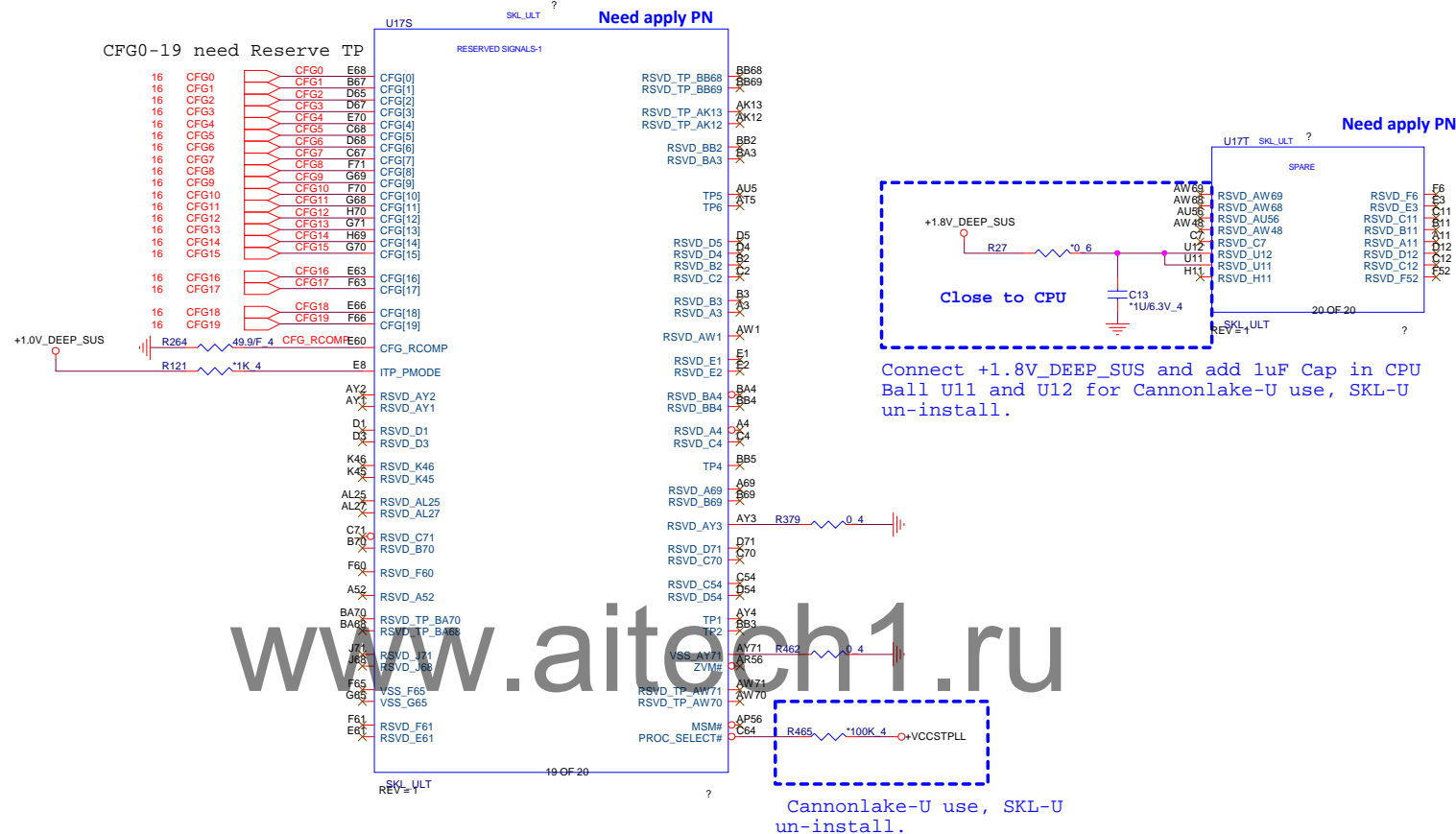


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



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+1.0V_DEEP_SUS 13,15,16,35,36
+VCCSTPLL 2,4,5,6,36,37

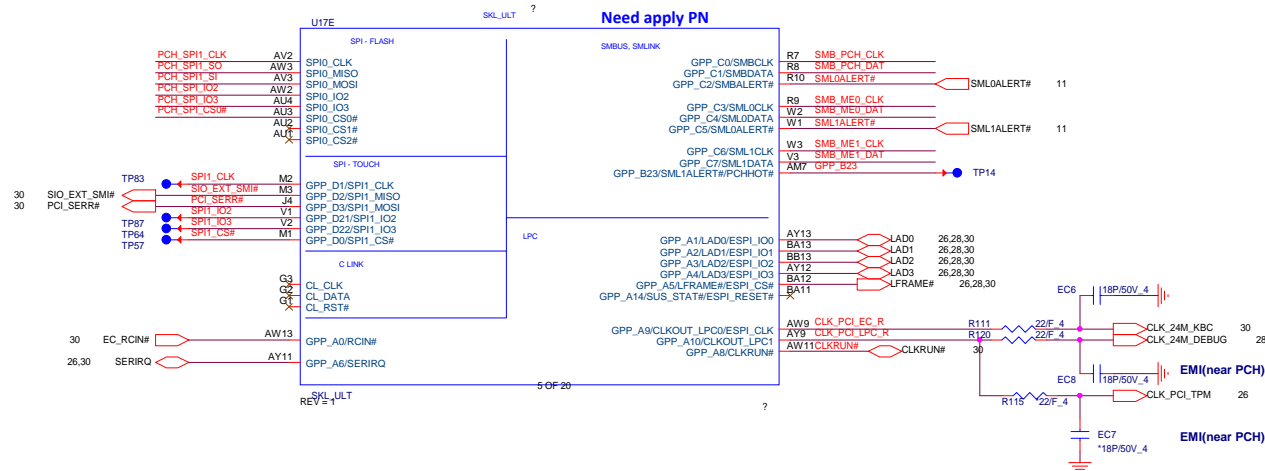


Processor Strapping

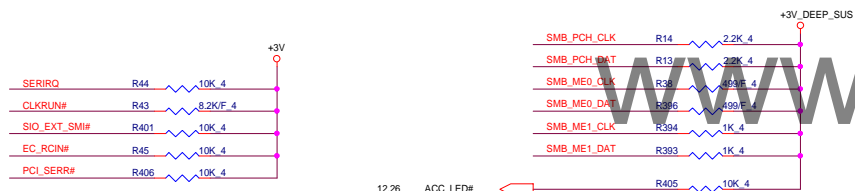
The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R466 ~1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R468 ~1K 4

+3V_DEEP_SUS 4,11,12,14,15,16,18
+3V 2,4,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
+3VSS 4,15,16,28,29,30,33,35,36,39



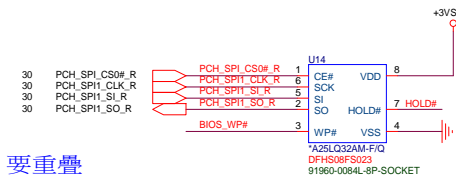
GPIO Pull UP



PCH SPI ROM(CLG)

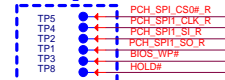
Vender	Size	P/N
EON	8MB	AKE3EZNO0Q1 (EN25QH64-104HIP)
Winbond	8MB	AKE3EPF0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

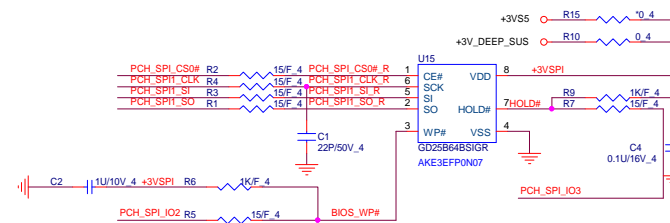


U14 & U15 footprint 要重疊

Need place to TOP

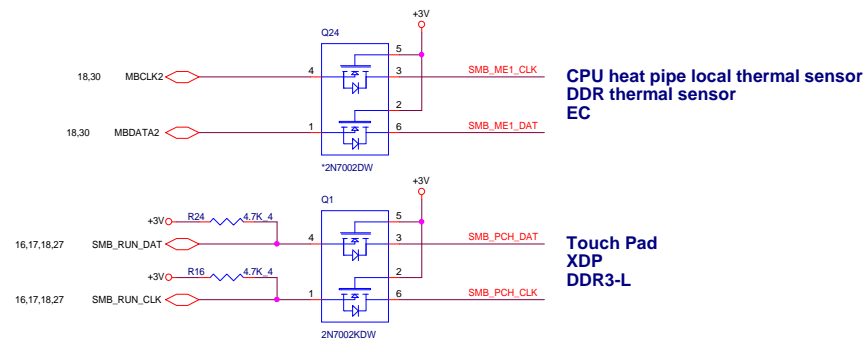


PCH SPI ROM(CLG)



R1/R2/R3/R4/R5/R7 close to U15 pin

SMBus/Pull-up(CLG)



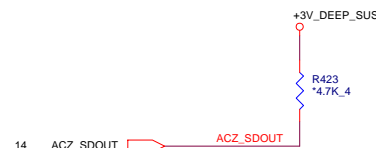
+3V_DEEP_SUS 4,10,12,14,15,16,18
+3V 2,4,10,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39

Functional Strap Definitions

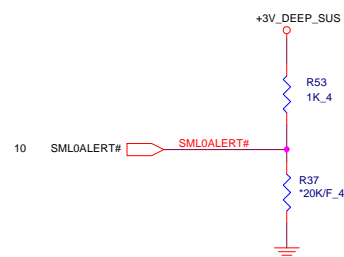
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



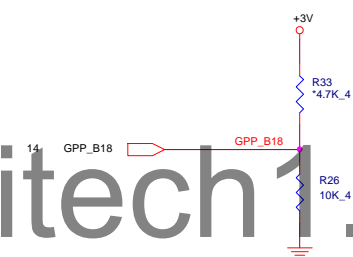
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



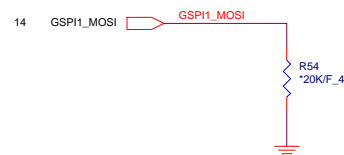
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



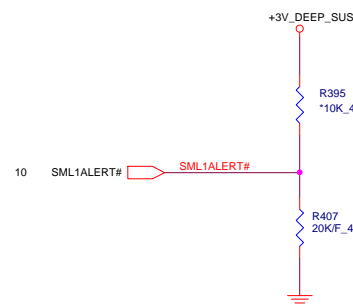
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

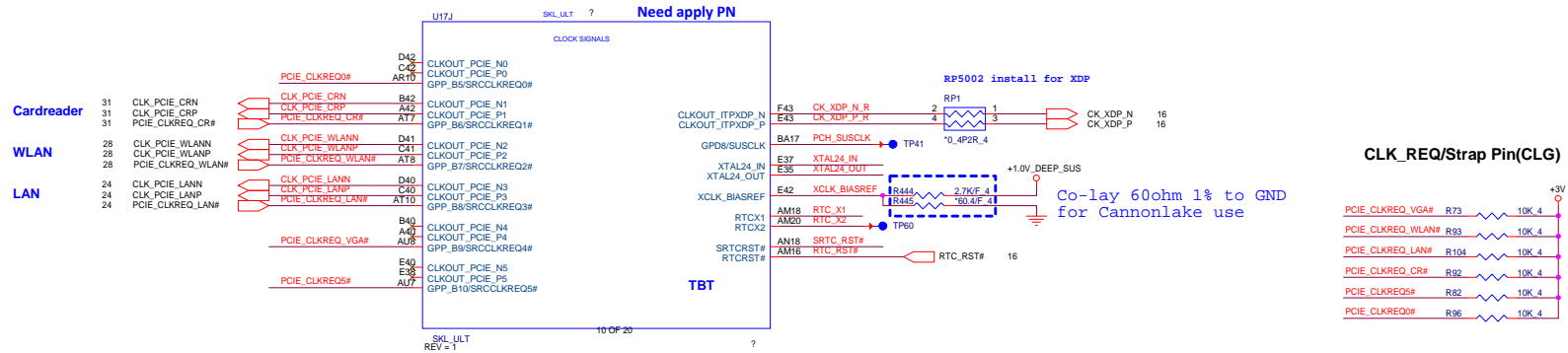


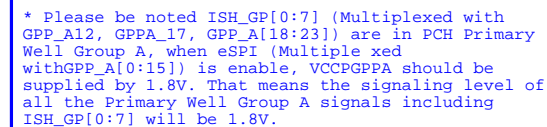
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



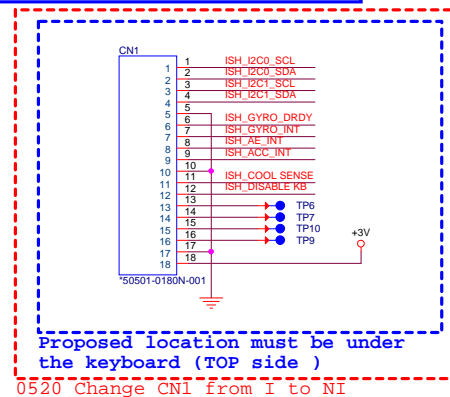
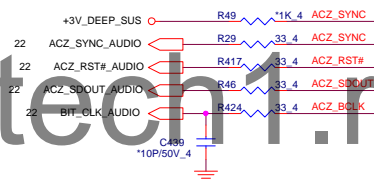
No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

+3V_RTC_2 4,15
 +3V_RTC 4,15,27,28,32
 +3V 2,4,10,11,12,14,15,16,17,18,20,21,22,23,24,25,26,27,29,30,31,37,39
 +1.0V_DEEP_SUS 9,15,16,35,36




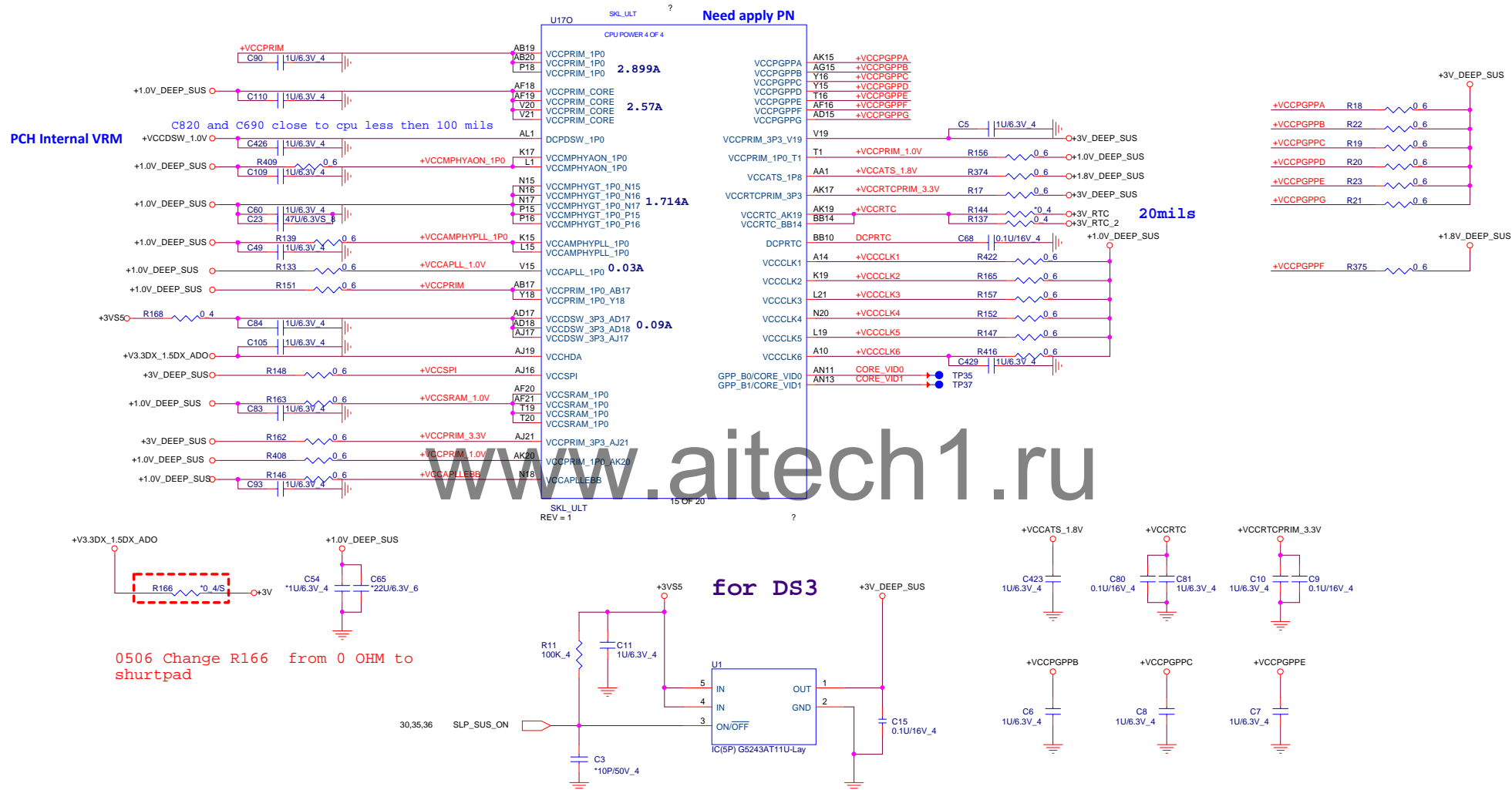


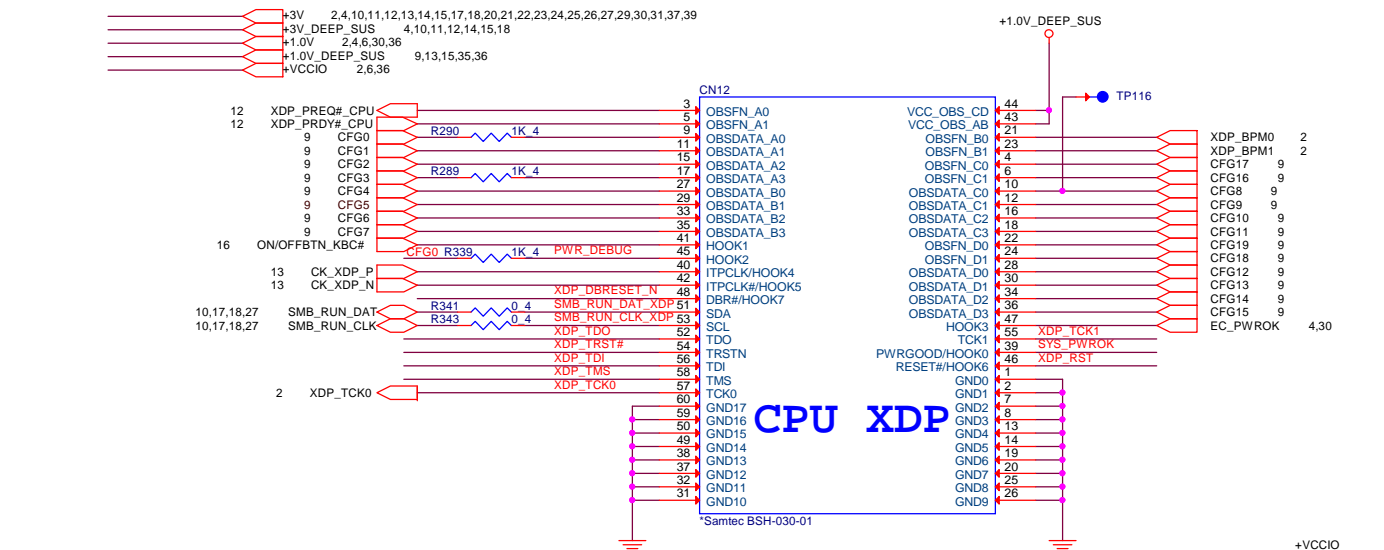
HDA Bus(CLG)



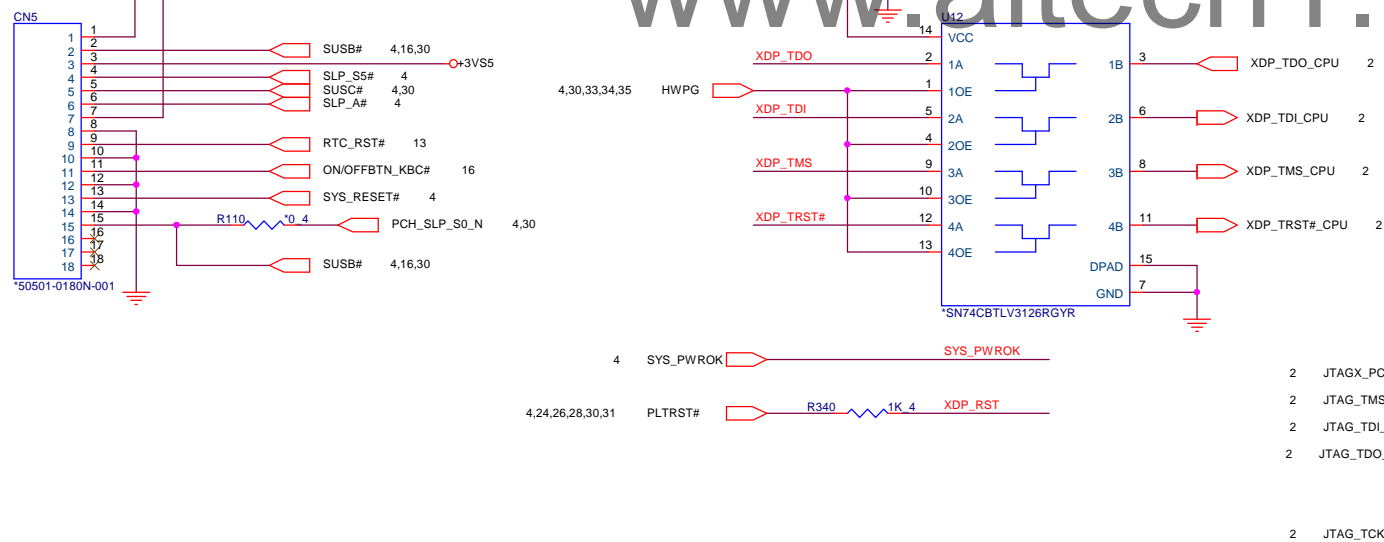
The diagram illustrates the timing and connections for the U17G component. It is divided into two main sections: **ACZ** (left) and **AUDIO** (right). The **ACZ** section shows signals like **ACZ_SYNC**, **ACZ_BCLK**, **ACZ_SDOUT**, **ACZ_SDINO**, **ACZ_RST#**, **SSP2_SFRM**, **SSP2_SCLK**, **SSP2_TXD**, **SSP2_RXD**, **GPP_D19**, **GPP_D20**, **GPP_D17**, **GPP_D18**, and **ACZ_SPKR**. The **AUDIO** section shows signals like **HDA_SYNCI2S0_SFRM**, **HDA_BLKI2S0_SCLK**, **HDA_SDOII2S0_TXD**, **HDA_SDOII2S0_RXD**, **HDA_SDI1I2S1_RXD**, **HDA_RST#I2S1_SCLK**, **GPP_D23I2S_MCLK**, **I2S1_SFRM**, **I2S1_TXD**, **GPP_F1I2S2_SFRM**, **GPP_F0I2S2_SCLK**, **GPP_F2I2S2_TXD**, **GPP_F3I2S2_RXD**, **GPP_D19/DMIC_CLK0**, **GPP_D20/DMIC_DATA0**, **GPP_D17/DMIC_CLK1**, **GPP_D18/DMIC_DATA1**, **GPP_B14/SPKR**, **GPP_G0/SD_CMD**, **GPP_G1/SD_DATA0**, **GPP_G2/SD_DATA1**, **GPP_G3/SD_DATA2**, **GPP_G4/SD_DATA3**, **GPP_G5/SD_CMD**, **GPP_G6/SD_CLK**, **GPP_G7/SD_TXD**, **GPP_A17/SD_PWR_EN/H5/GPT**, **GPP_A16/SD_1PB_SEL**, **SD_RCOMP**, and **GPP_F23**. The **SDIO/SDXC** section shows signals like **GPP_G0/SD_CMD**, **GPP_G1/SD_DATA0**, **GPP_G2/SD_DATA1**, **GPP_G3/SD_DATA2**, **GPP_G4/SD_DATA3**, **GPP_G5/SD_CMD**, **GPP_G6/SD_CLK**, **GPP_G7/SD_TXD**, **GPP_A17/SD_PWR_EN/H5/GPT**, and **GPP_A16/SD_1PB_SEL**. The **SD_RCOMP** section shows signals like **SD_RCOMP** and **GPP_F23**. The **SDIO/SDXC** section shows signals like **SDIO/SDXC** and **GPP_A17/SD_PWR_EN/H5/GPT**. The **SD_RCOMP** section shows signals like **SD_RCOMP** and **GPP_F23**. The **SDIO/SDXC** section shows signals like **SDIO/SDXC** and **GPP_A17/SD_PWR_EN/H5/GPT**. The **SD_RCOMP** section shows signals like **SD_RCOMP** and **GPP_F23**.

	PROJECT : Y62P/Y63P Quanta Computer Inc.		
	Size Custom	Document Number 14 – SKYPAKE 19/20 (GPIO)	Rev 1A
Date: Wednesday, May 20, 2015		Sheet 14 of 42	



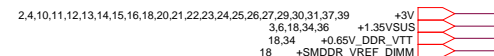


APS



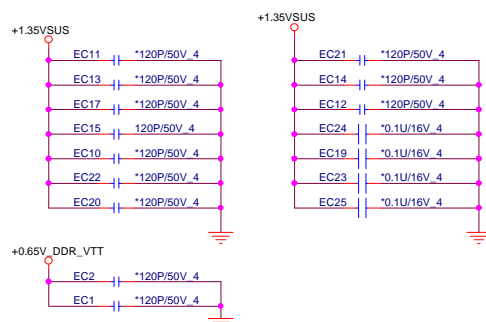
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size	Document Number	Rev
	16 -- HSW XDP & APS	1A
Date: Wednesday, May 20, 2015	Sheet 16 of 42	



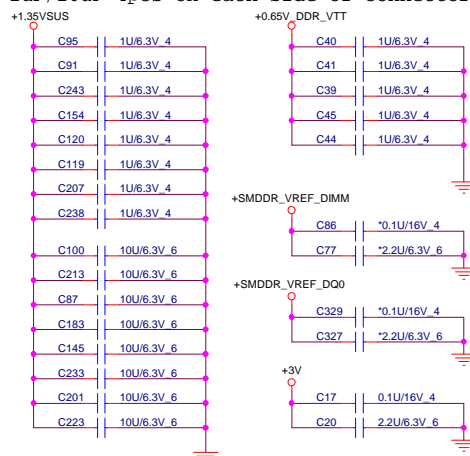
DQ53	174	M A DQ54
DQ54	176	M A DQ51
DQ55	181	M A DQ61
DQ56	183	M A DQ60
DQ57	191	M A DQ59
DQ58	193	M A DQ65
DQ59	180	M A DQ37
DQ60	182	M A DQ56
DQ61		

For EMI RESERVE

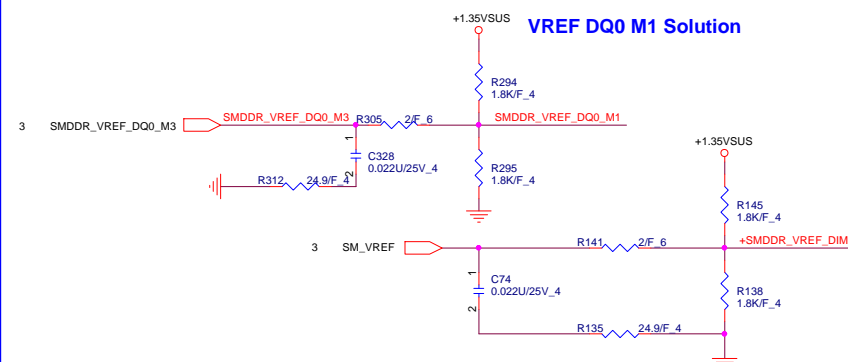


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

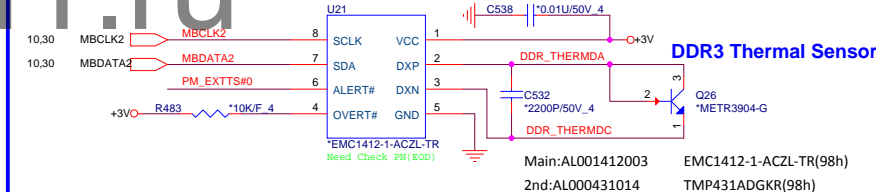


VREF DQ0 M1 Solution



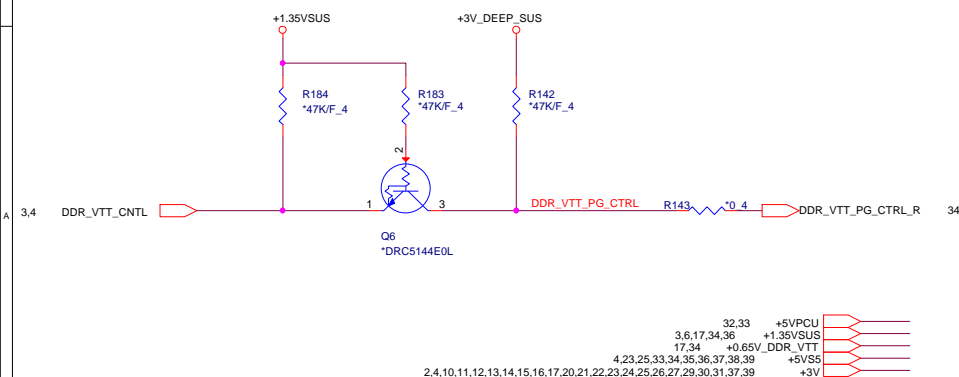
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size Custom	Document Number 17 -- DDR3 DIMMO-STD(4.0H)	Rev 1A
Date: Wednesday, May 20, 2015	Sheet 17 of 42	



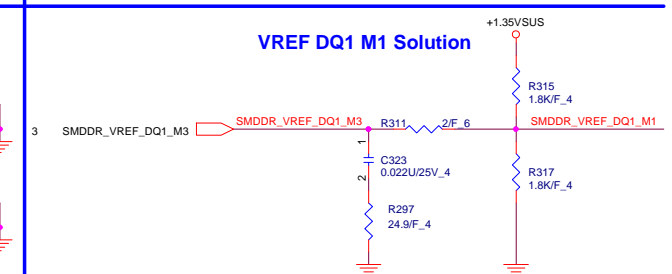
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

VREF DQ1 M1 Solution



The schematic diagram illustrates the power plane for the i35VSUS module, featuring several decoupling capacitors and their associated values:


- +1.35VSUS:**
 - C89: 1U/6.3V 4
 - C225: 1U/6.3V 4
 - C79: 1U/6.3V 4
 - C208: 1U/6.3V 4
 - C242: 1U/6.3V 4
 - C126: 1U/6.3V 4
 - C185: 1U/6.3V 4
 - C230: 1U/6.3V 4
 - C152: 10U/6.3V 6
 - C184: 10U/6.3V 6
 - C86: 10U/6.3V 6
 - C156: 10U/6.3V 6
 - C203: 10U/6.3V 6
 - C241: 10U/6.3V 6
 - C122: 10U/6.3V 6
 - C101: 10U/6.3V 6
- +0.65V_DDR_VTT:**
 - C22: 1U/6.3V 4
 - C43: 1U/6.3V 4
 - C46: 1U/6.3V 4
 - C47: 1U/6.3V 4
 - C37: 10U/6.3V 6
 - C18: 0.1U/16V 4
 - C19: 2.2U/6.3V 6
- +SMDDR_VREF_DIMM:**
 - C76: *0.1U/16V 4
 - C82: *2.2U/6.3V 6
- +SMDDR_VREF_DQ1:**
 - C334: *0.1U/16V 4
 - C336: *2.2U/6.3V 6



PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size Custom	Document Number 18 -- DDR3 DIMM-RVS(4.0H)	Rev 1A
Date: Wednesday, May 20, 2015	Sheet 18 of	42

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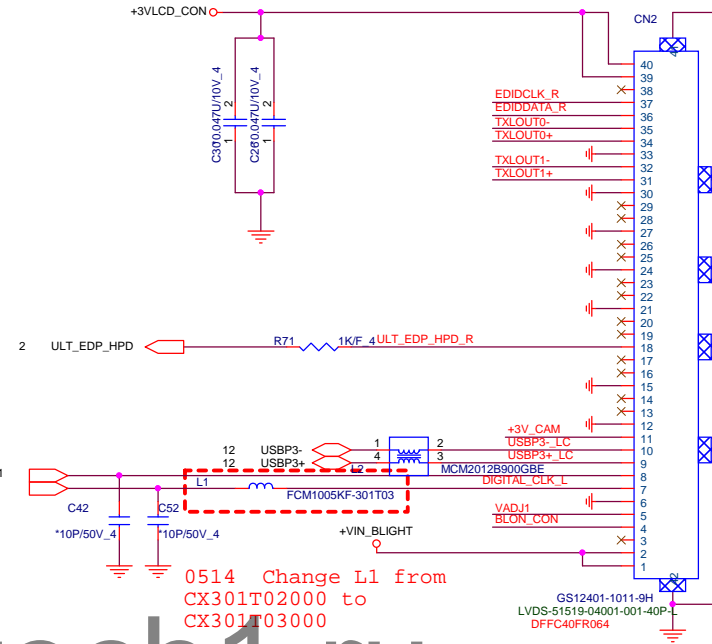
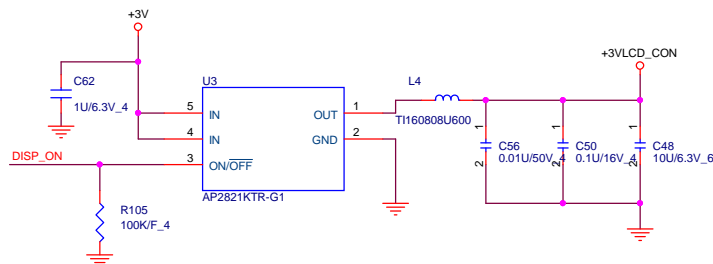
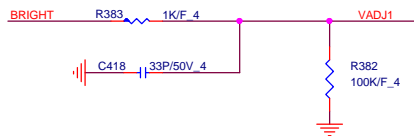
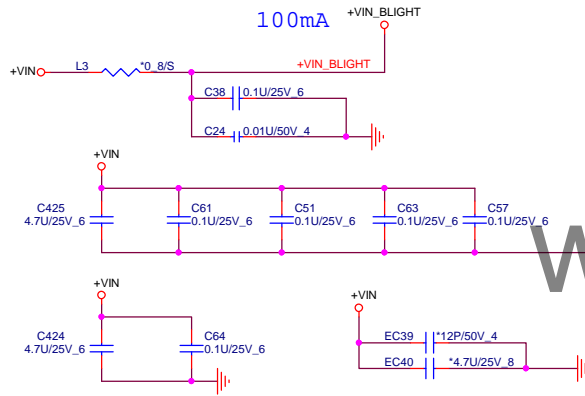
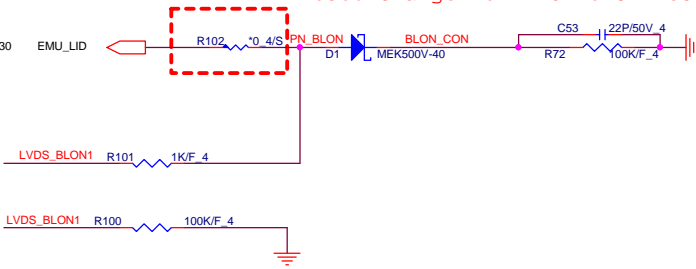
		PROJECT : Y62P/Y63P	
		Quanta Computer Inc.	
Size Custom	Document Number RTD2136		Rev 1A
Date: Wednesday, May 20, 2015		Sheet	19 of 42

LID Switch

0506 Change R102 from 0 OHM to shurtpad

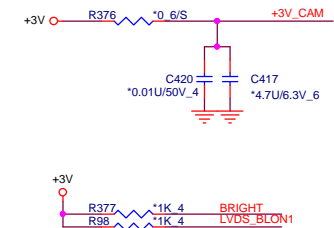
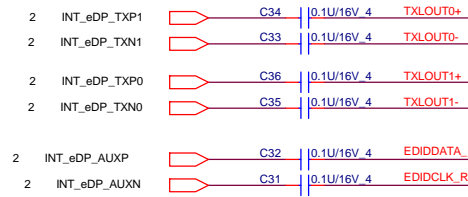
eDP Conn.

20

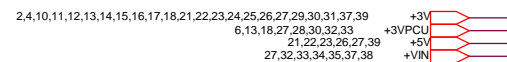


0514 Change L1 from CX301T02000 to CX301T03000

0506 Change CN2 footprint from lvds-50671-04041-001-40p-1 to LVDS-51519-04001-001-40P-L



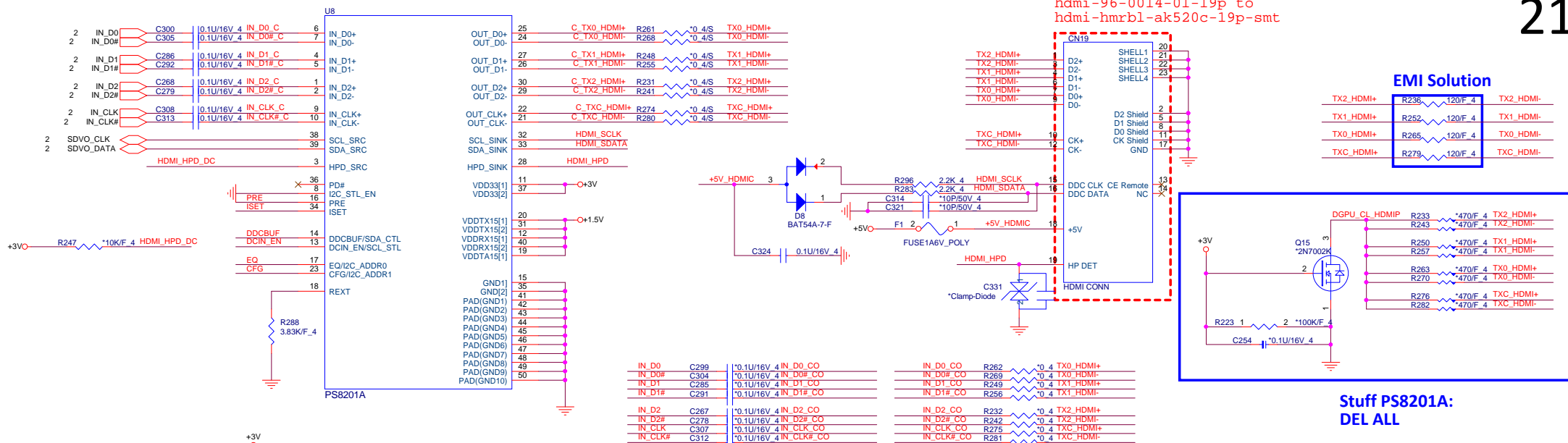
0506 Change R99, R106 from 0 OHM to shurtpad



PROJECT : Y62P/Y63P
Quanta Computer Inc.

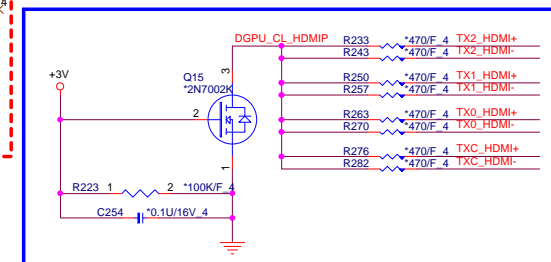
Size Custom	Document Number	Rev 1A
LCD CONN/LID/CAM		
Date: Wednesday, May 20, 2015	Sheet 20 of 42	

0415 Change CN19 footprint from
hdmi-96-0014-01-19p to
hdmi-hmrbl-ak520c-19p-smt



EMI Solution

TX2_HDMI+	R236	*120/F_4	TX2_HDMI-
TX1_HDMI+	R252	*120/F_4	TX1_HDMI-
TX0_HDMI+	R265	*120/F_4	TX0_HDMI-
TXC_HDMI+	R279	*120/F_4	TXC_HDMI-



Stuff PS8201A:
DEL ALL

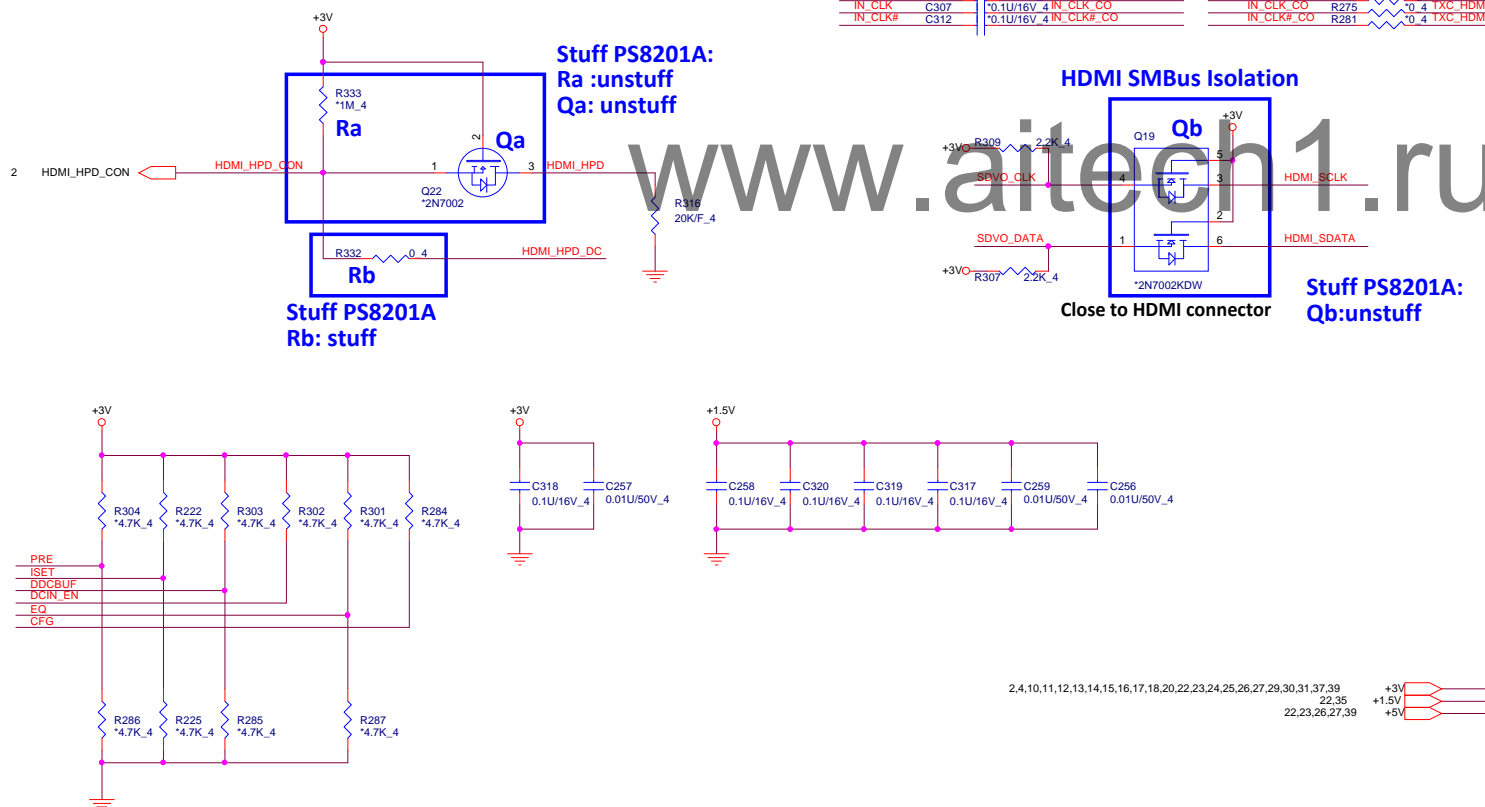
Stuff PS8201A:

Ra :unstuff
Qa: unstuff

HDMI SMBus Isolation

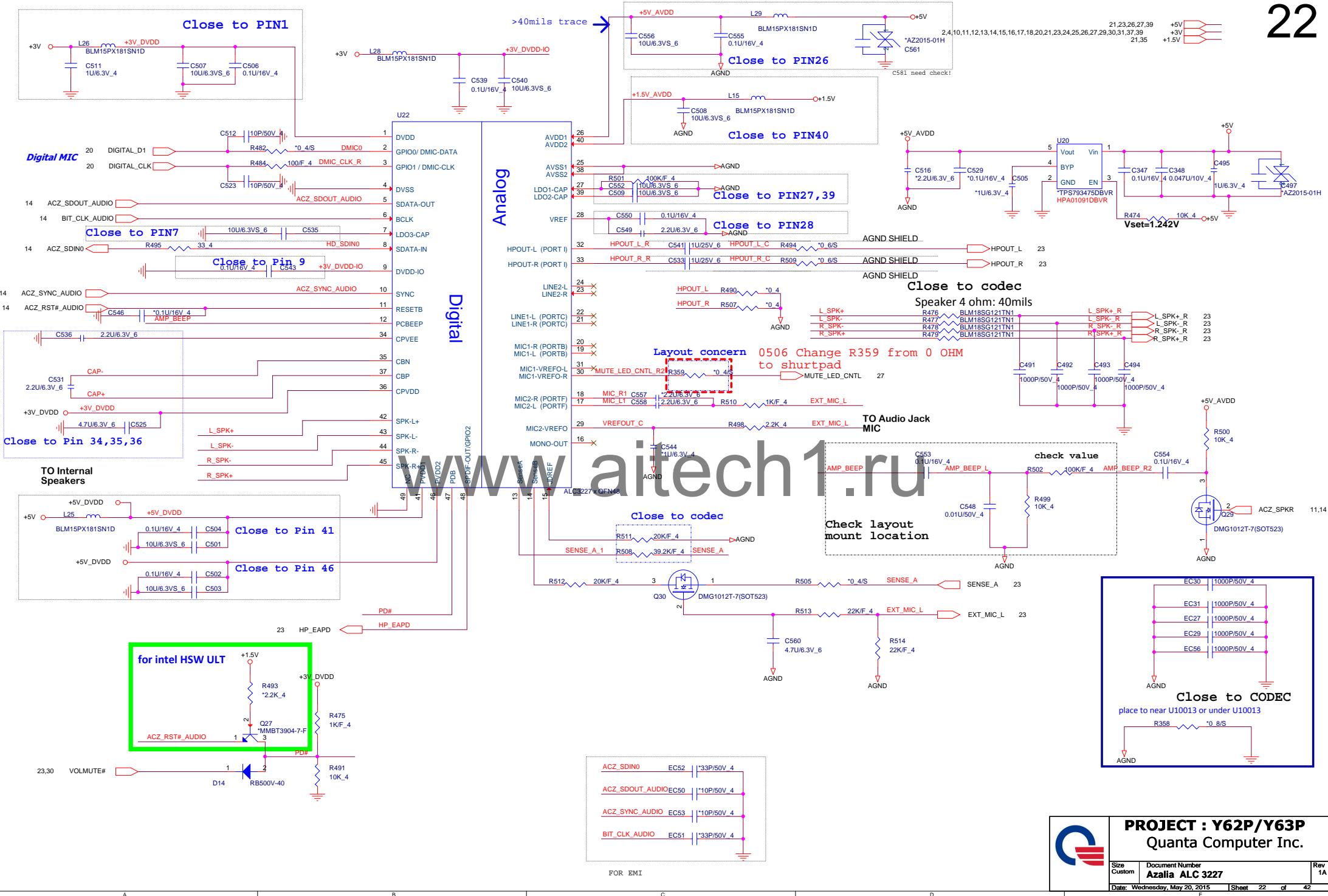
Close to HDMI connector

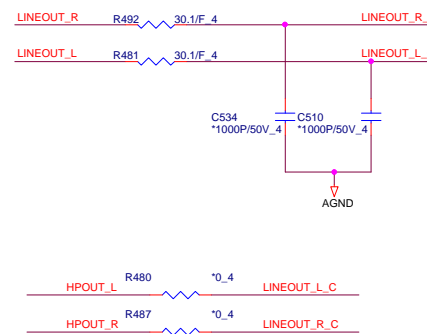
Stuff PS8201A:
Qb:unstuff



2,4,10,11,12,13,14,15,16,17,18,20,22,23,24,25,26,27,29,30,31,37,39
22,35
22,23,26,27,39

+3V
+1.5V
+5V

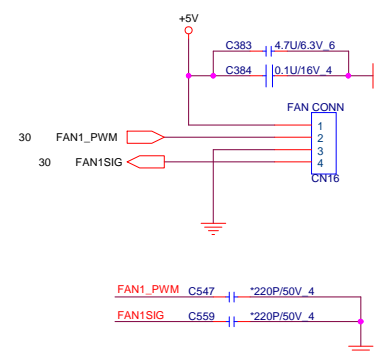
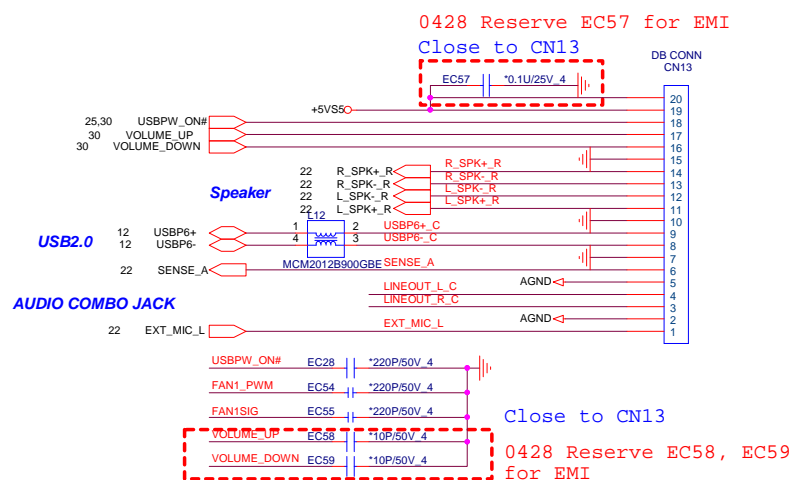




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Audio Board

FAN



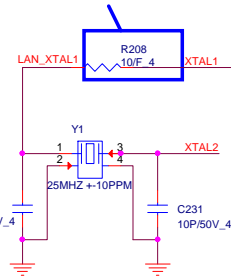
2,4,10,11,12,13,14,15,16,17,18,20,21,22,24,25,26,27,29,30,31,37,39
21,22,26,27
4,25,33,34,35,36,37,38,



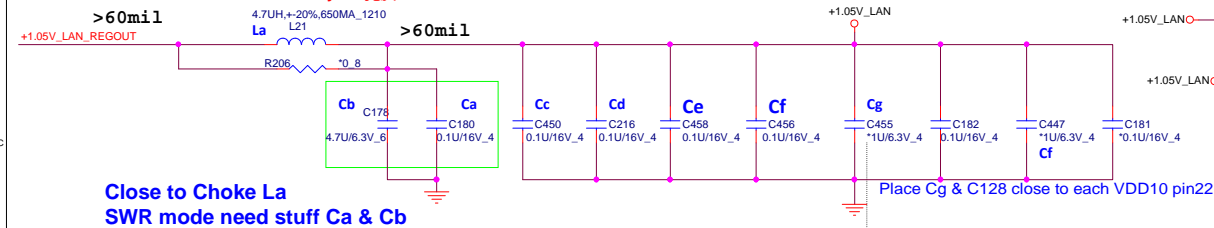
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size Custom	Document Number Audio/AMP HPA022642RTJR	Rev 1.
Date: Wednesday, May 20, 2015		Sheet 23 of 42

For EMI 0 ~ 22 ohm

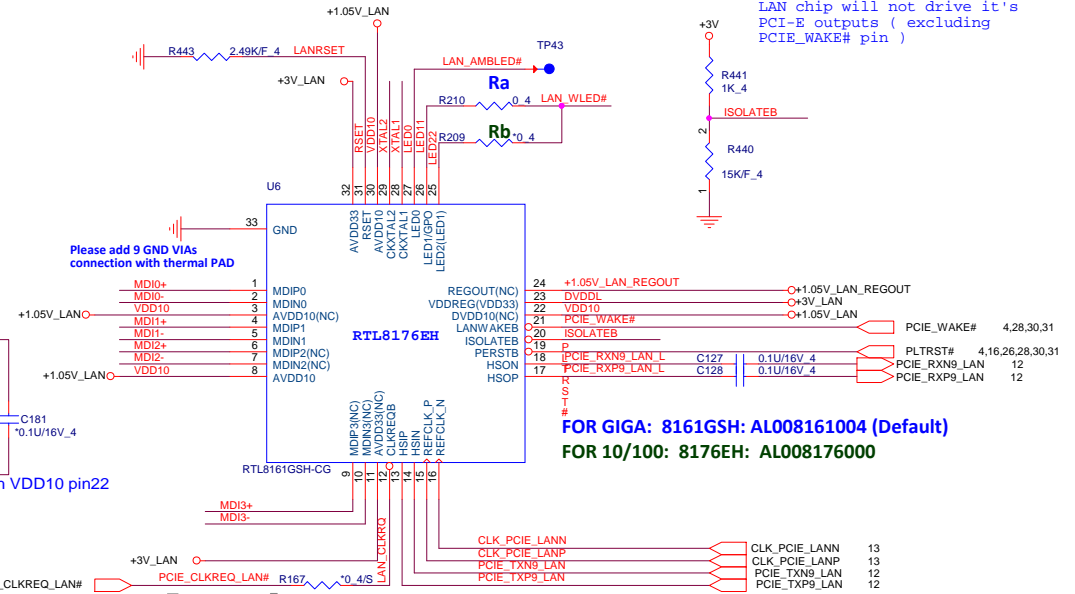


Trace<30 mil
Width > 60 mil
>60mil



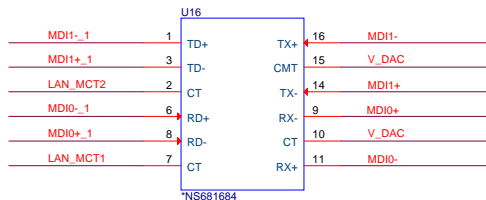
Close to Choke La
SWR mode need stuff Ca & Cb

For GbE
* Place Cg close to each VDD10 pin-- 22 (reserve)



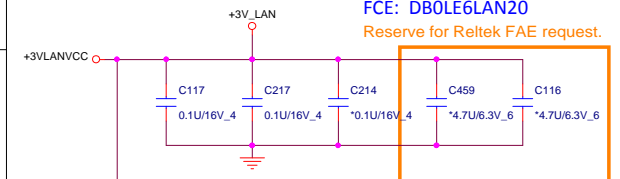
FOR GIGA: 8161GSH: AL008161004 (Default)
FOR 10/100: 8176EH: AL008176000

10/100 only

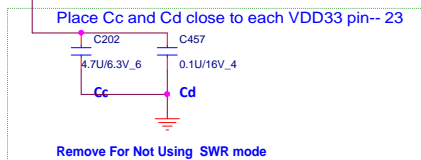


BOT: DBOLE6LAN00
FCE: DBOLE6LAN20

Reserve for Reltek FAE request.



close to each VDD33 pin-- 11, 32

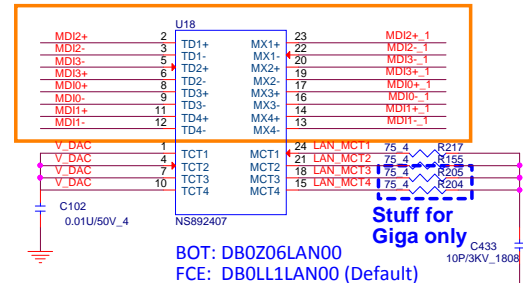


Remove For Not Using SWR mode

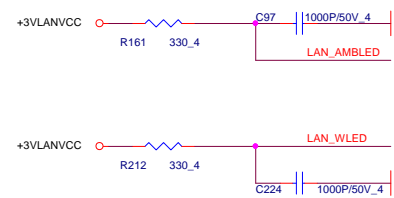
2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,25,26,27,29,30,31,37,39

+3V
+3V+3V
+3V

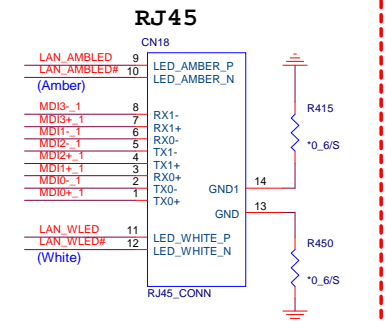
Giga only
Swap pin for Layout



BOT: DB0Z06LAN00
FCE: DB0LL1LAN00 (Default)



LAN conn

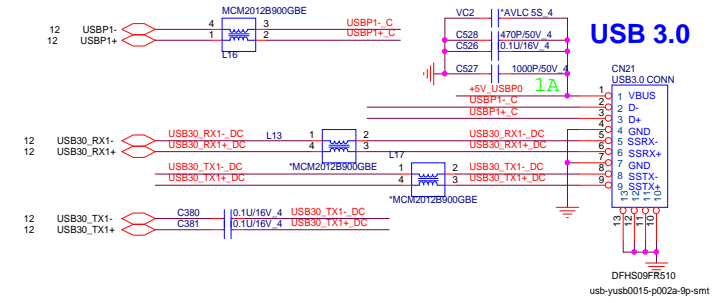
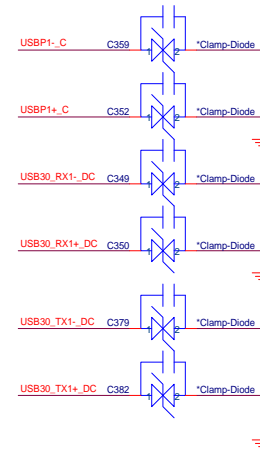
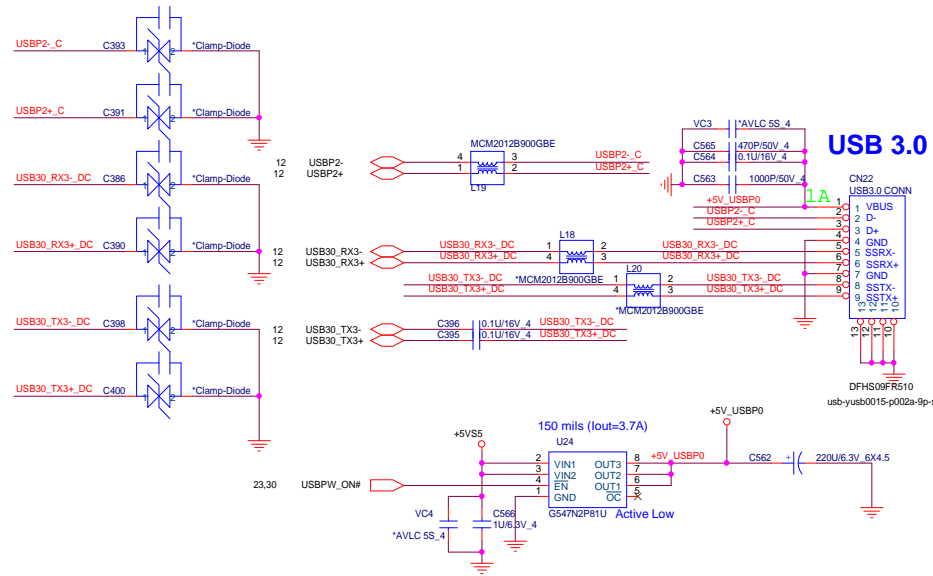


0224
Need check P/N

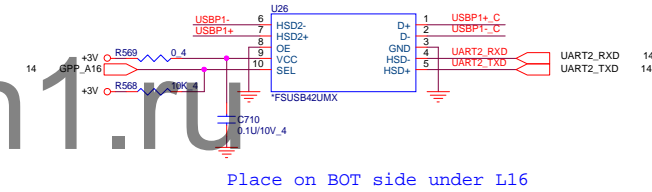


PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size Custom	Document Number RTL 8161/RJ45	Rev 1A
Date: Wednesday, May 20, 2015	Sheet 24 of 42	



UART for DEBUG



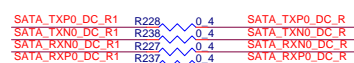
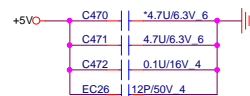
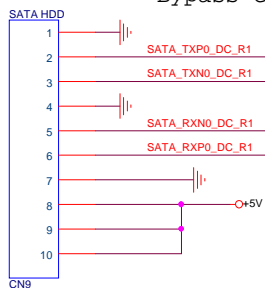
Place on BOT side under L16

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5VSS 4.23,33,34,35,36,37,38,39
+3V 2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,26,27,29,30,31,37,39

SATA HDD Connector(Cable type)

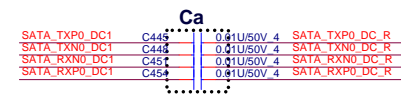
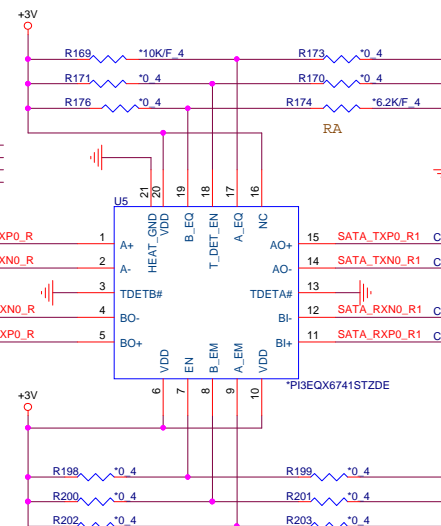
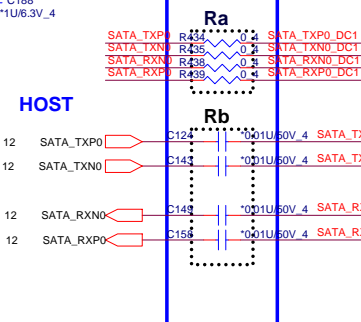
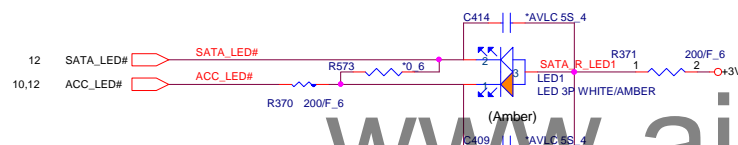
Bypass CAP close conn



LED1	PN	
Dual Color	BEWY0009ZA0	stuff R370, unstuff R573
Single Color	BEWH0046Z00	stuff R573, unstuff R370

SATA Re-driver

Ra & Rb need place close

**SATA LED**

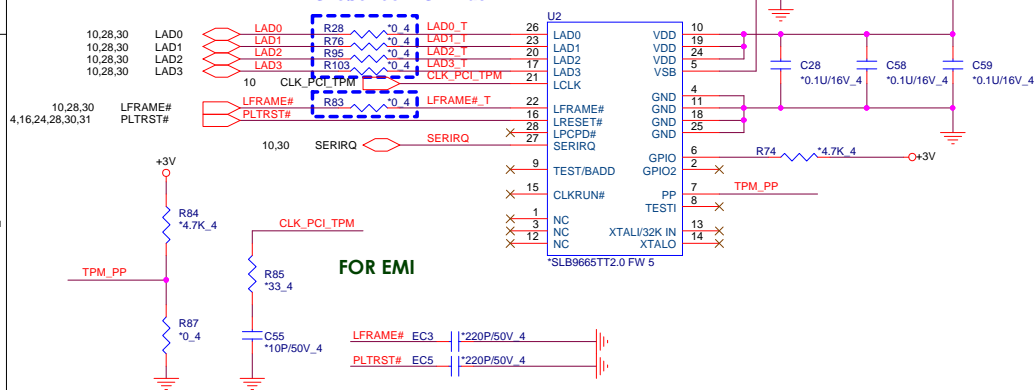
SATA re-driver IC
stuff Rb,Cb , unstuff Ra,Ca
unstuff SATA re-driver IC
stuff Ra,Ca , unstuff Rb,Cb

TPM (2.0)

Address

	BADD
HIGH	4EH/4F (default)

Close to EC Side



2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,27,29,30,31,37,39
21 22 23 27

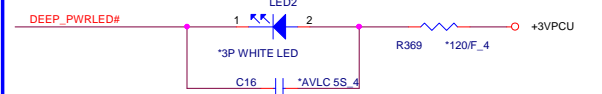


PROJECT : Y62P/Y63P
Quanta Computer Inc.

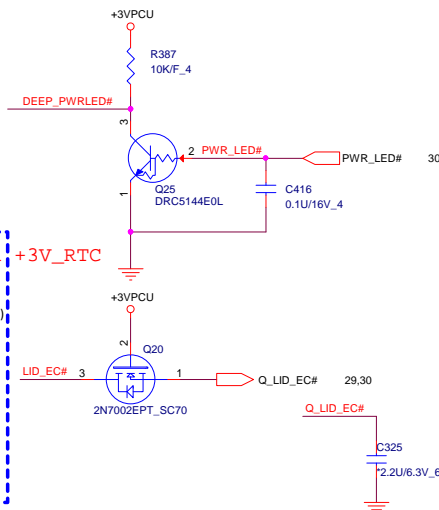
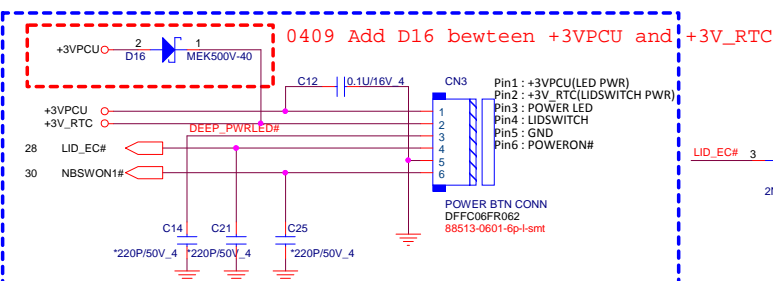
Size Custom	Document Number HDD/mSATA/FAN/LED	Rev 1A
Date: Wednesday, May 20, 2015	Sheet 26 of	42

Power Button Connector

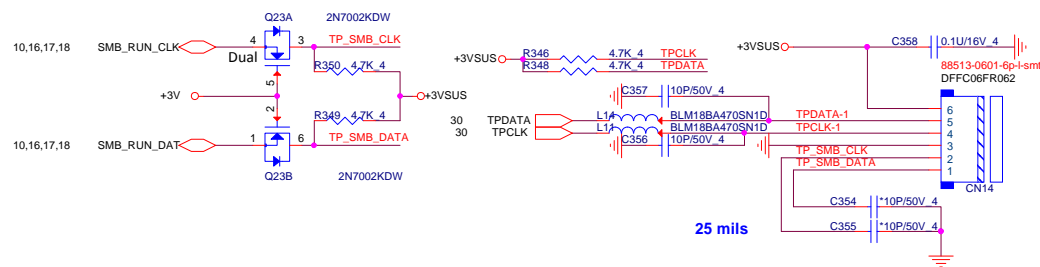
PWR LED Clamshell (Y61) only



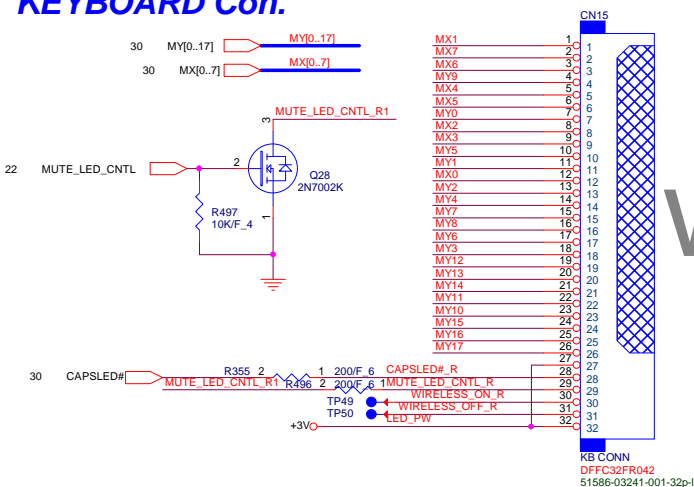
Pin define is different
Power Board does not shared with Y6x !!



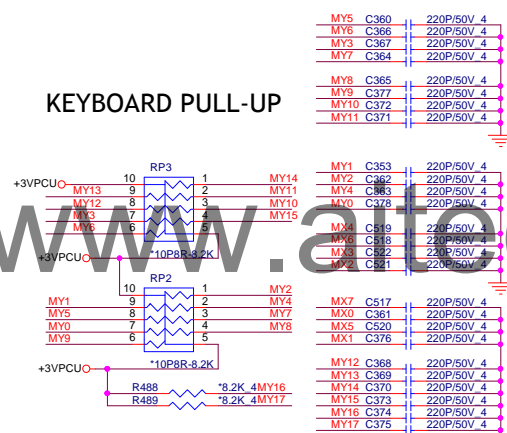
Touch Pad Connector



KEYBOARD Con.

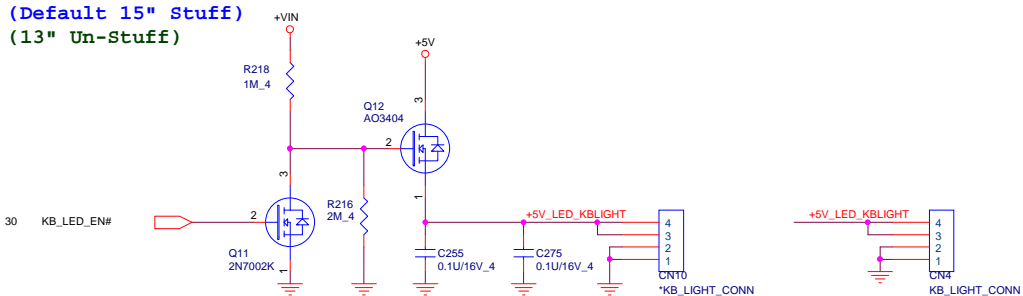


KEYBOARD PULL-UP

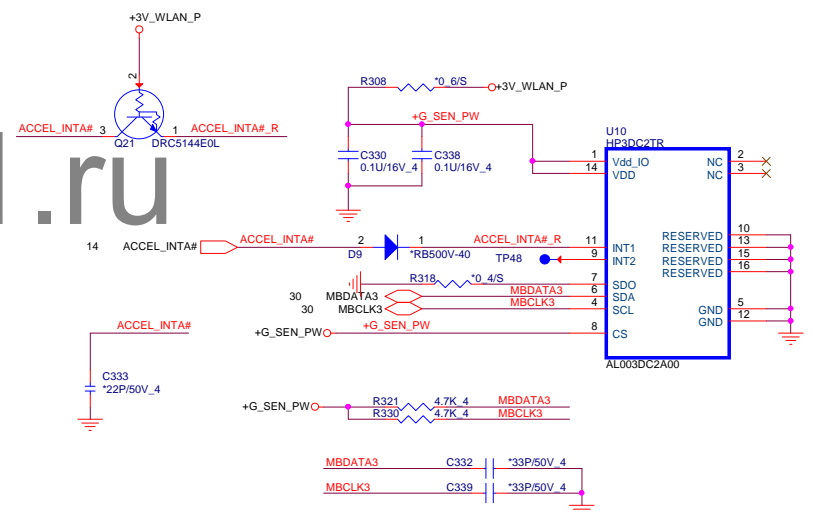


15" KB backlight only

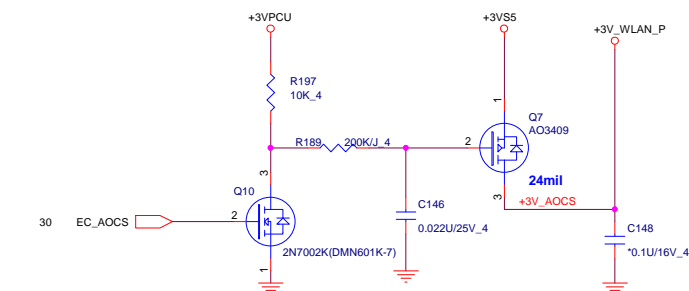
(Default 15" Stuff)
(13" Un-Stuff)



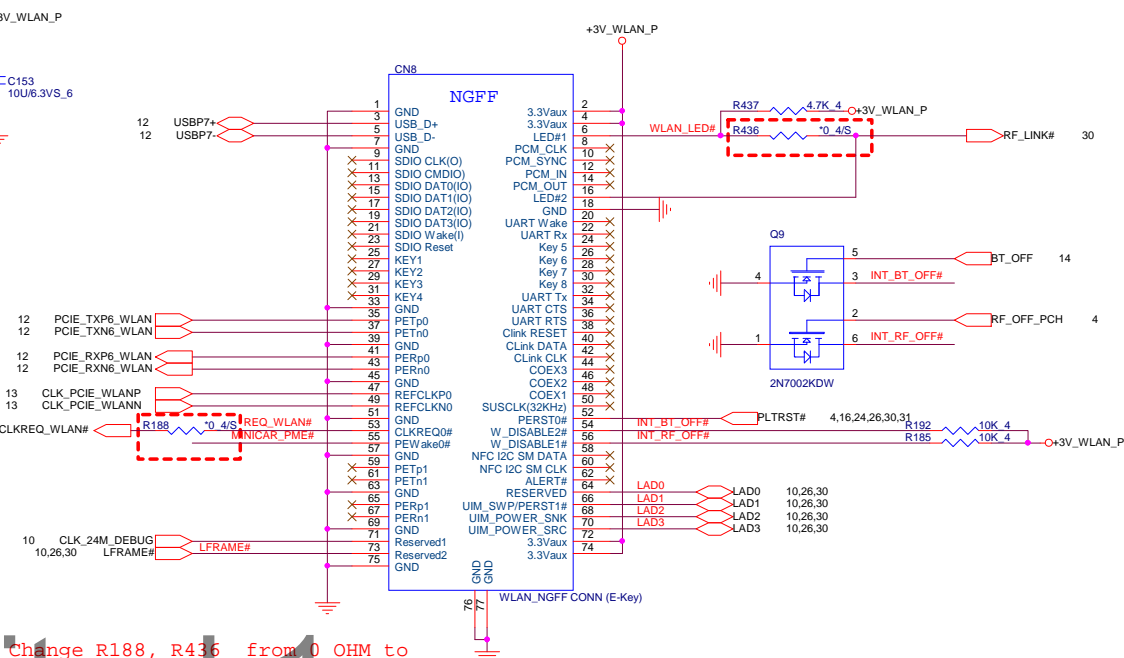
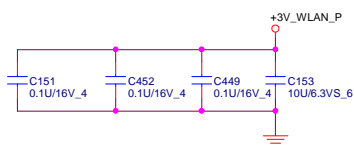
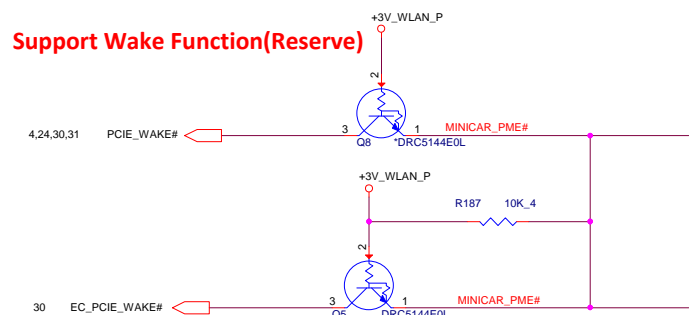
Accelerometer Sensor



Mini Card
WLAN/BT(Optional)



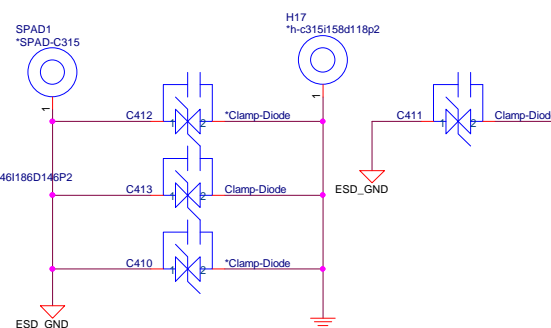
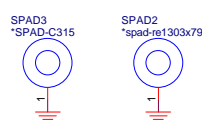
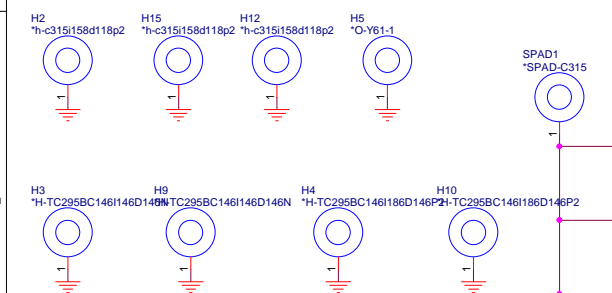
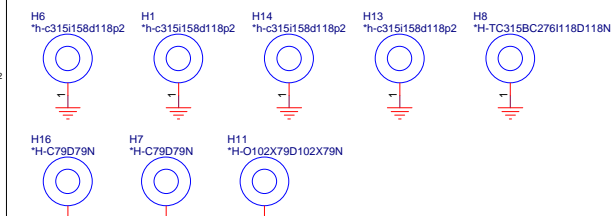
Support Wake Function(Reserve)



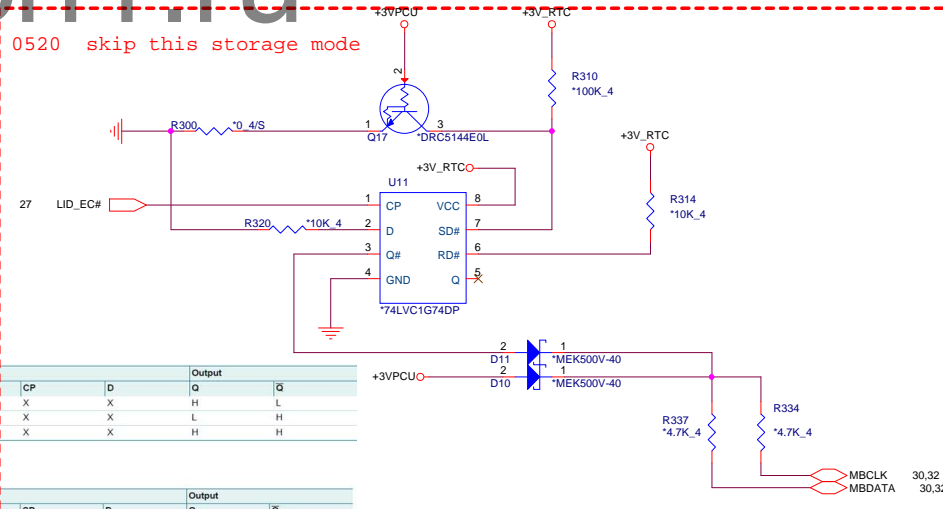
0506 Change R188, R436 from 0 OHM to shurtpad

0506 Change R188, R436 from 0 OHM to shortpad

Hole



```
0520 skip this storage mode
```



Input				Output	
SD	RD	CP	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

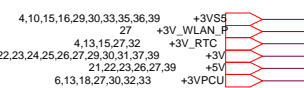
[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input		
SD	RD	CP
H	H	↑
H	H	↑

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

Input		Output			
SD	RD	CS	D	$D_{0,1}$	$D_{2,3}$
H	H	↑	L	L	H
H	H	↑	L	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition



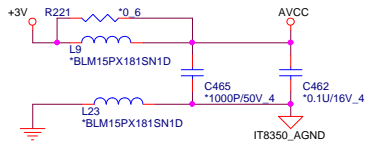
PROJECT : Y62P/Y63P
Quanta Computer Inc.

Size Custom	Document Number WLAN/G-Sensor/G-CLK/TS	Rev 1A
Date: Wednesday, May 20, 2015	Sheet 28 of 42	

2,4,10,11,12,13,14,15,16,17,18,20,21,22,23,24,25,26,27,30,31,37,39
4,10,15,16,28,30,33,35,36,39

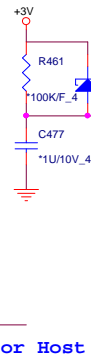
+3V
+3VSS

20MIL



20MIL

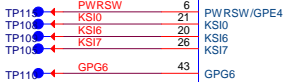
U19
*IT8350E_LQFP-48



USB for Host



USB



GPIO

IT8350E
LQFP-48

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Reserved TX/RX for debugging

if no use ADC function,
please pull down to GND
SMINTx for sensor interrupt

GPG2 can't floating

External crystal is must be item
when USB func. is used !

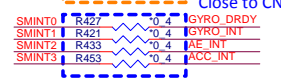
32.768kHz clock lines:

- If possible, please avoid using any through-hole.
- Please make the trace length short, and the trace width wide enough.
- The spacing to the closest neighbor should be wide enough.

Close to CN3



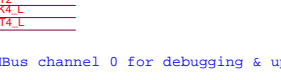
Close to U23



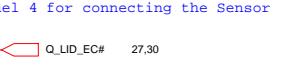
Close to U23



Close to U23



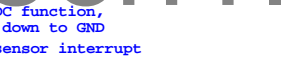
Close to U23



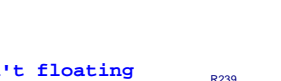
Close to U23



Close to U23



Close to U23



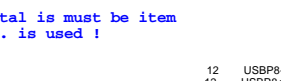
Close to U23



Close to U23



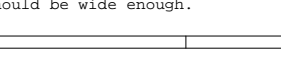
Close to U23



Close to U23



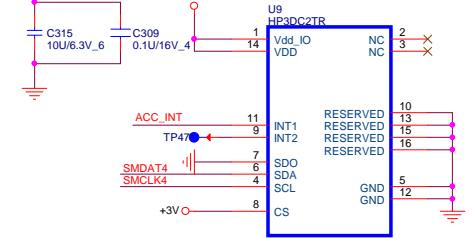
Close to U23



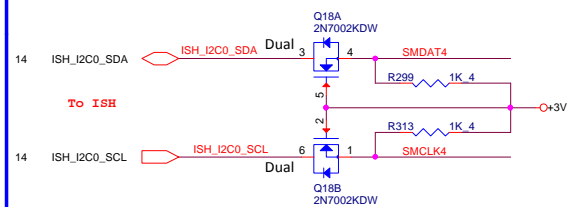
Close to U23

Accelerometer Sensor

Put it on MB side

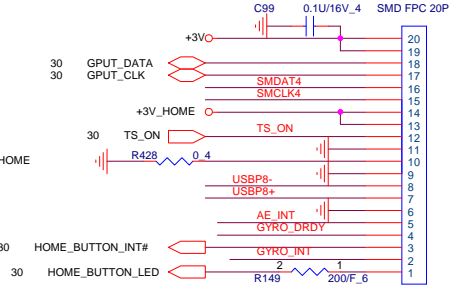
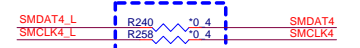


Close to U9



To Sensor Hub SMBUS

Close to U23



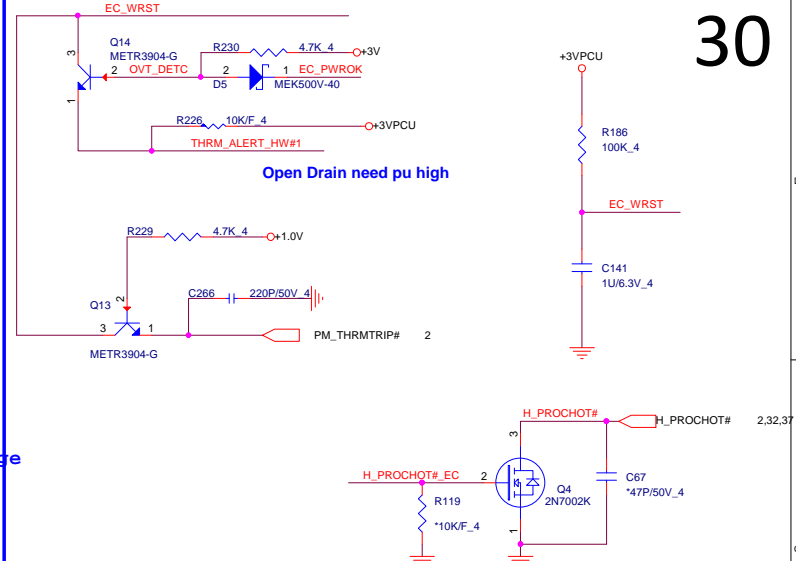
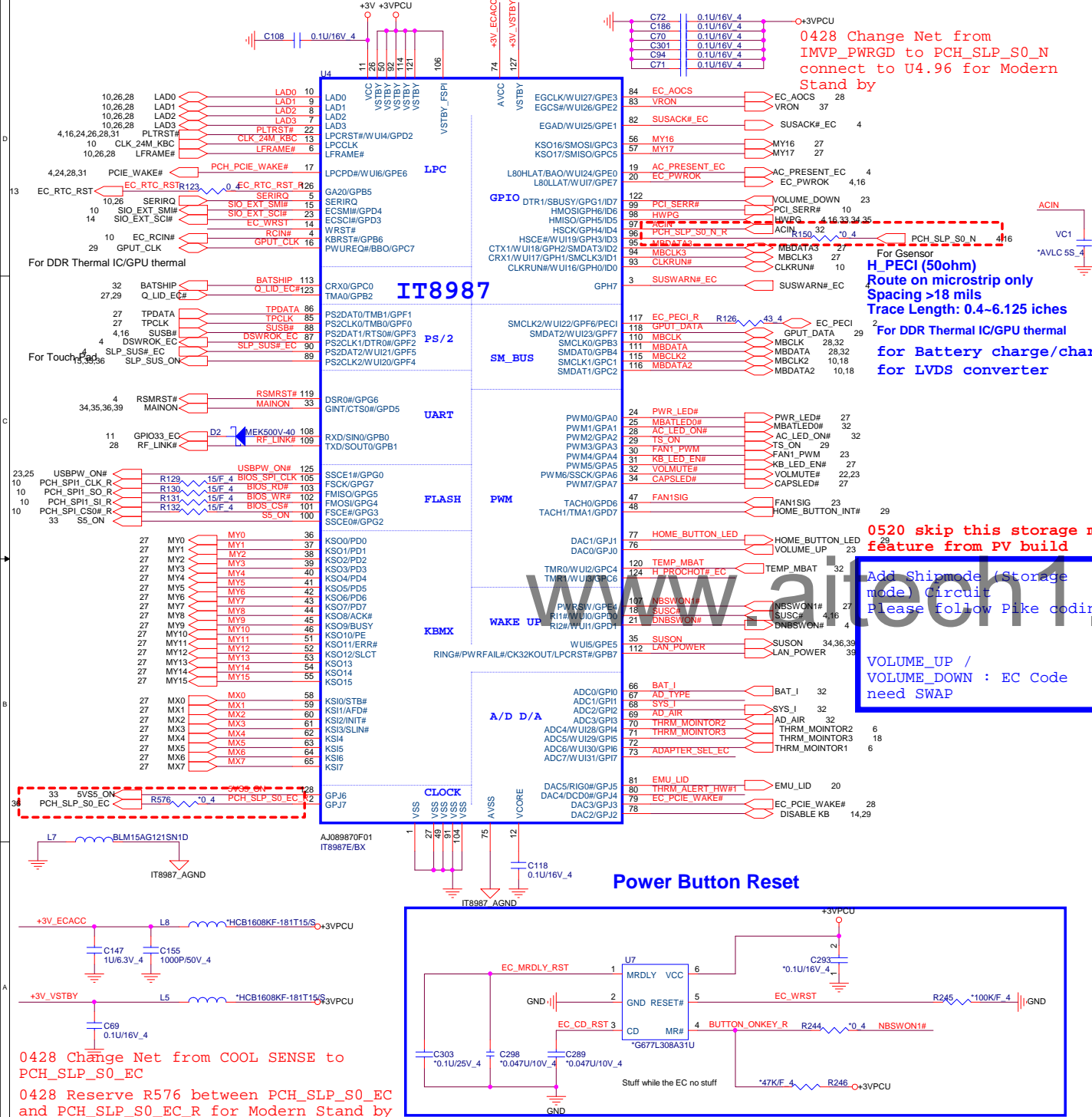
0415 Del TS Co-Lay CN6



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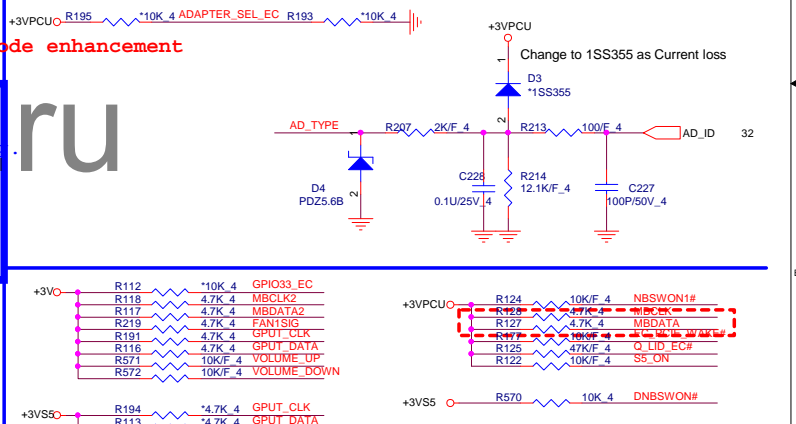
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0428 Change Net from
IMVP_PWRGD to PCH_SLP_S0_N
connect to U4.96 for Modern
Stand by

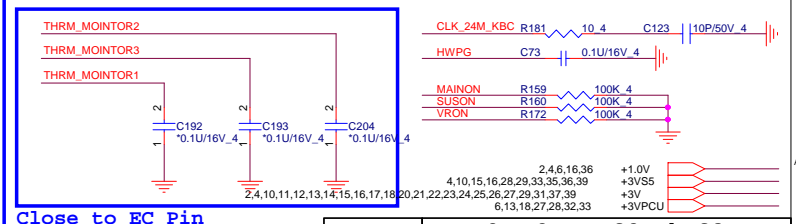


Adapter select for EC

adapter Type check



0520 Change R127, R128 from NI to I



Close to EC Pin

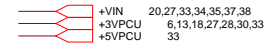
This pull-down resistor is less than 10k
form Pike(Y0D)
The circuit will fix leakage current when
EC during mirror code/HW initial process

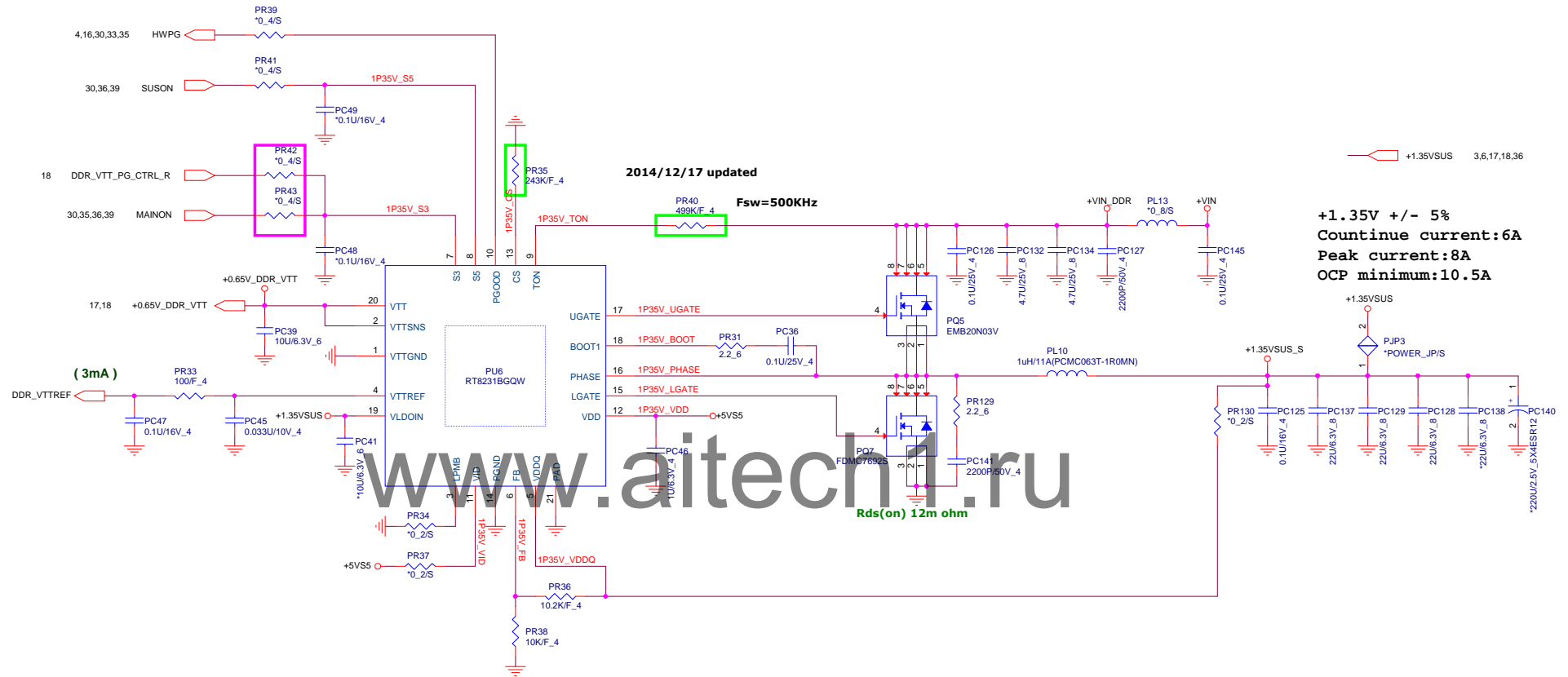


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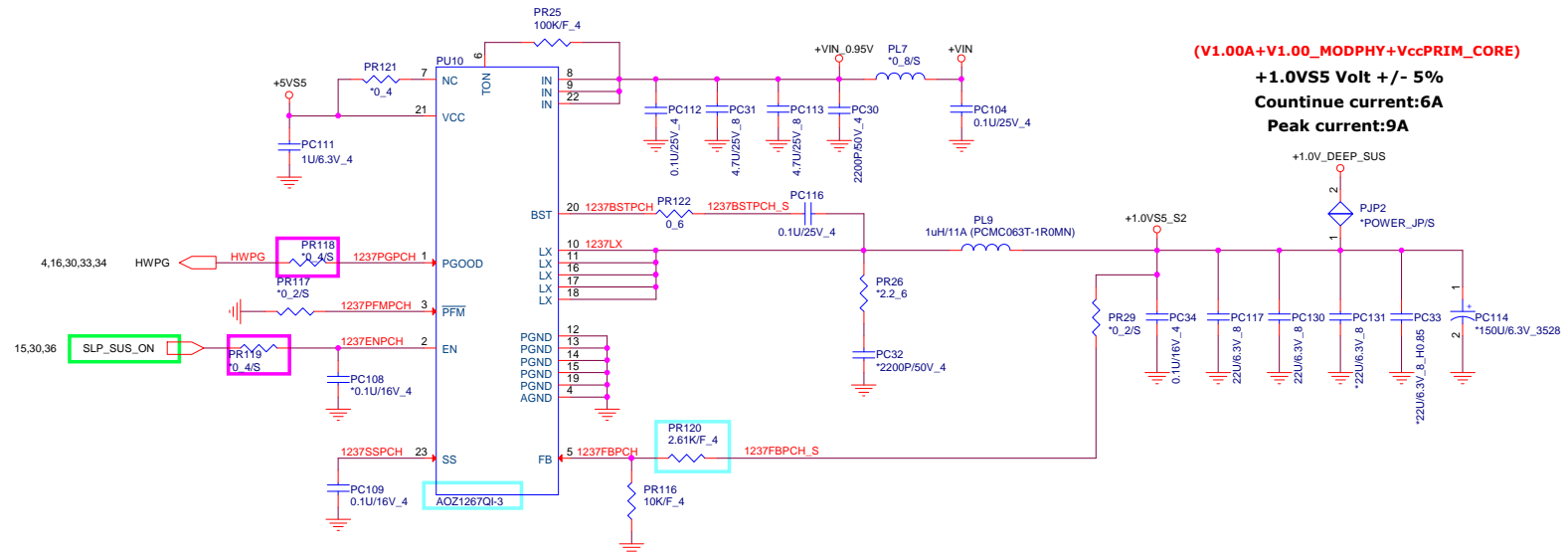
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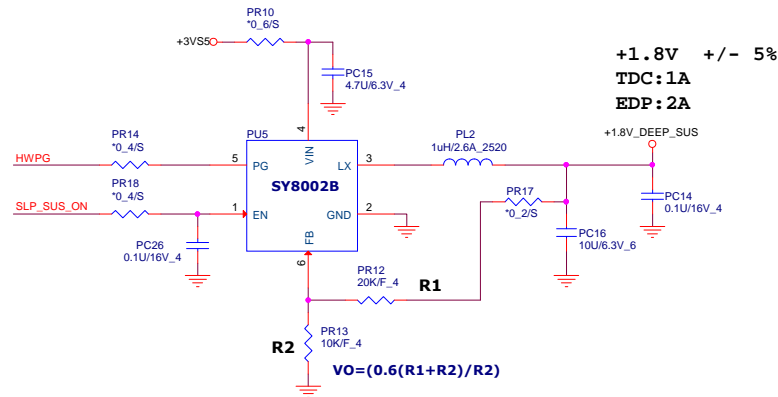




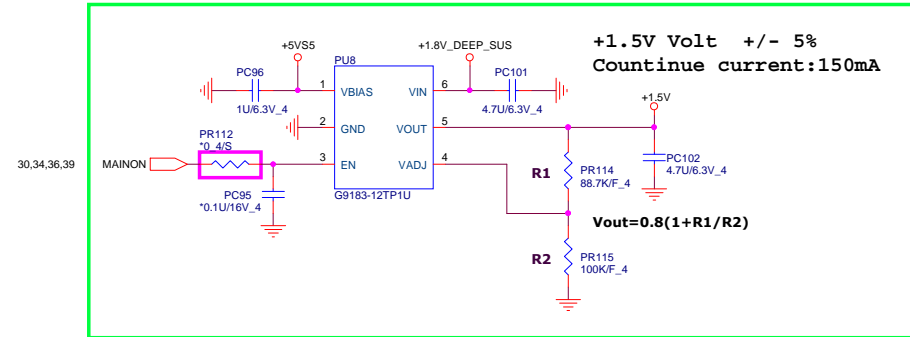
+VIN 20,27,32,33,34,37,38
 +3VS5 4,10,15,16,28,29,30,33,36,39
 +5VS5 4,23,25,33,34,36,37,38,39
 +1.0V_DEEP_SUS 9,13,15,16,36
 +1.8V_DEEP_SUS 9,15

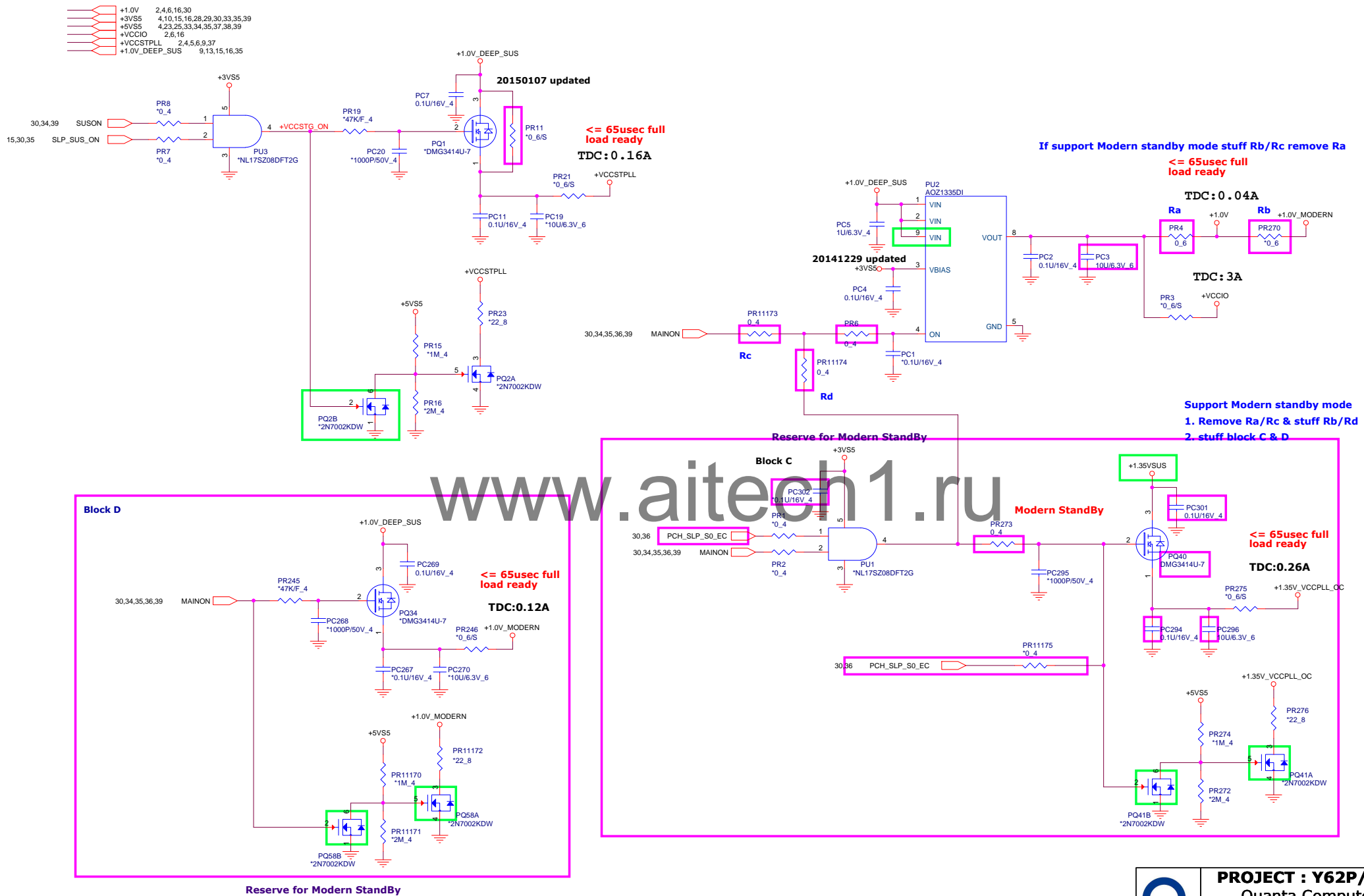


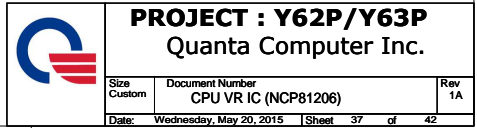
www.aitech1.ru

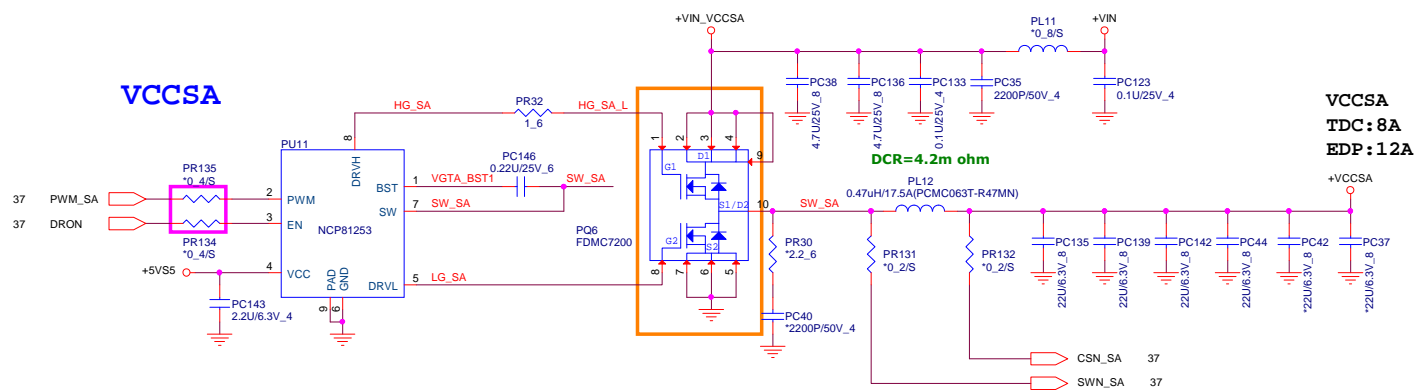


20150111 updated

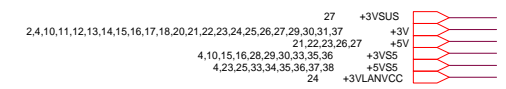


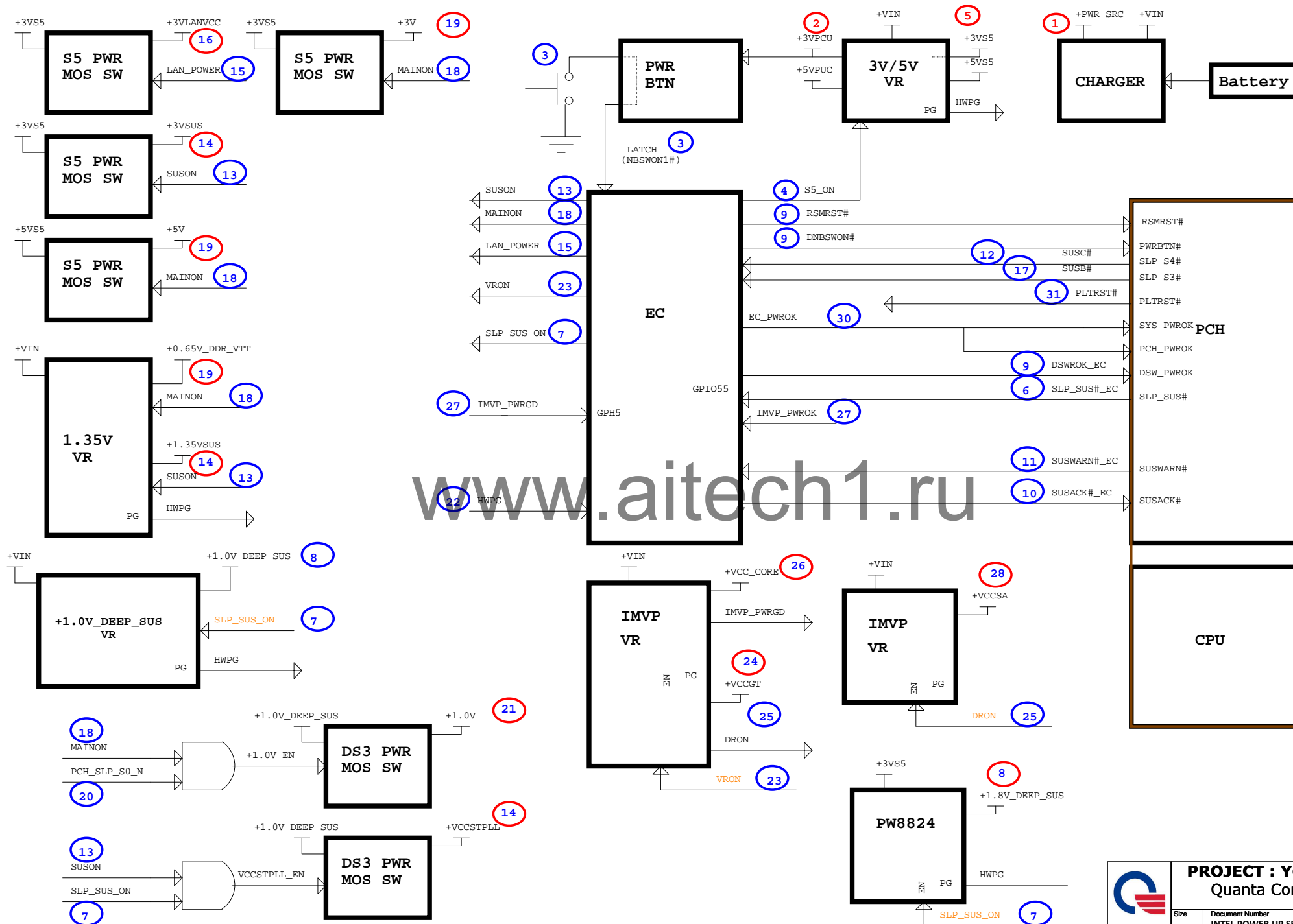


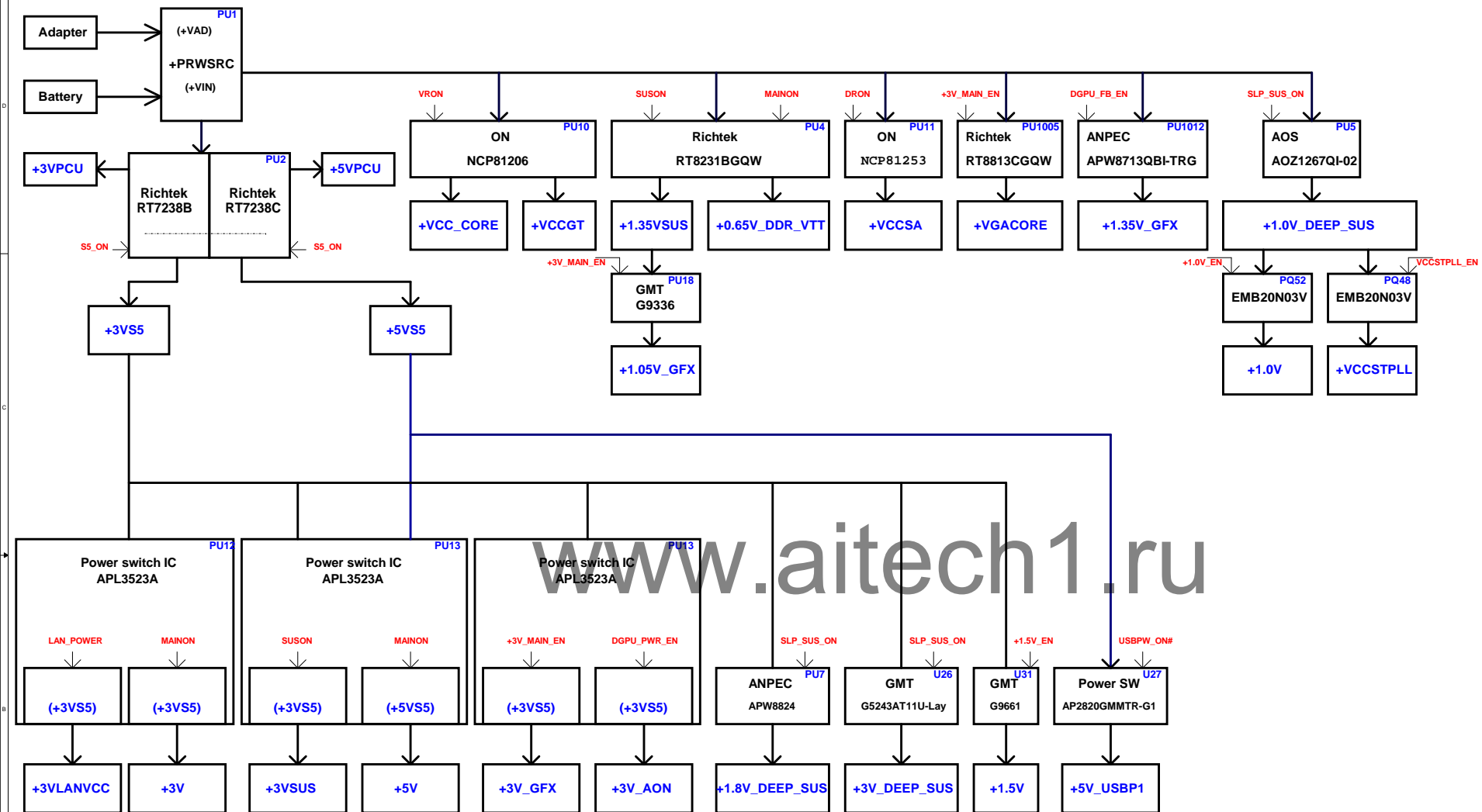


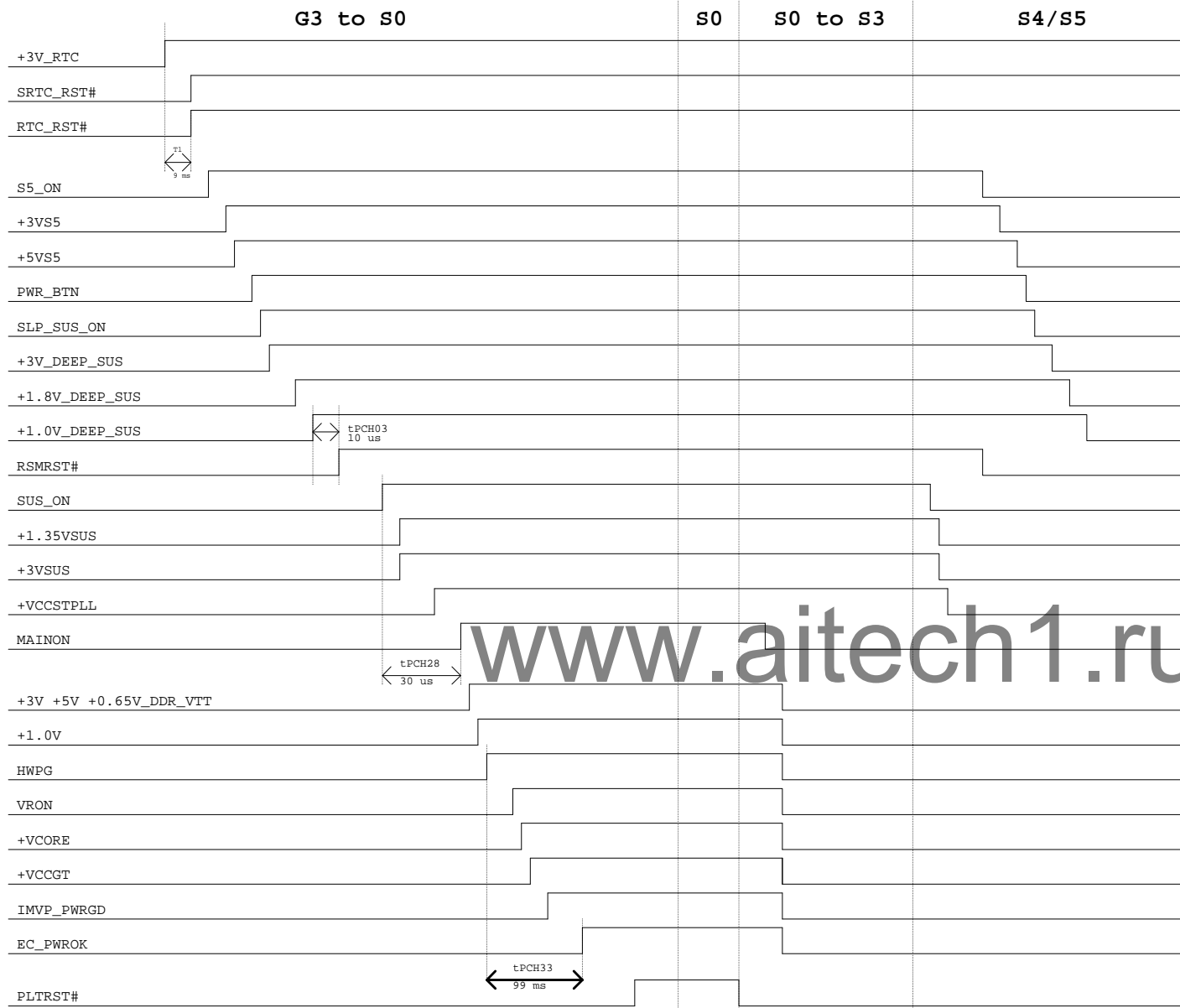


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